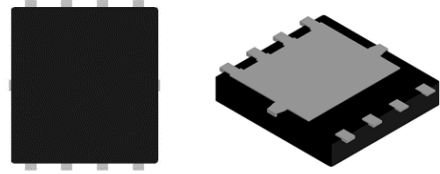


FEATURES

- Drain-Source Withstand Voltage: 60V
- Max. $R_{DS(on)}$: 8.5m Ω @ $V_{GS}=-10V$
13.3m Ω @ $V_{GS}=4.5V$
- Automotive applications
- AEC-Q101 Qualified
- Excellent ON resistance
- General footprint package PDFN5×6-8L
- 100% Rg and Avalanche tested
- MSL1

PRODUCT APPEARANCE


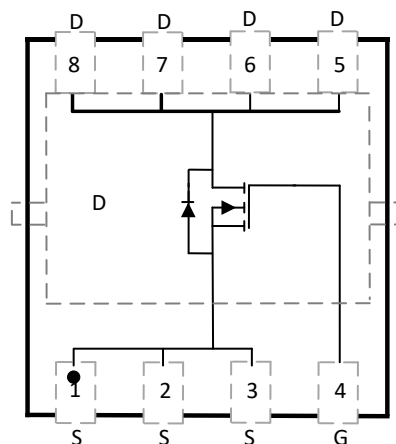
PDFN5×6-8L

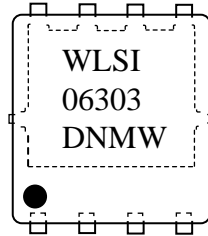
DESCRIPTION

The SNM067R9DNAQ is N-Channel enhancement MOS Field Effect Transistor. Uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use in high performance automotive DC-DC conversion, power switch and charging circuit. Standard Product SNM067R9DNAQ is in compliance with RoHS.

Applications:

- Automotive systems
- DC/DC converters
- Power supply converters circuit
- Load/Power Switching for portable device

PIN CONFIGURATION


MARKING


WLSI = Company (Group) Code
 06303 = Device Code
 DN = Special Code
 M = Month
 W = Week

LIMITING VALUES

Parameter	Symbol	Condition	Value	Unit
Drain-Source Voltage	V_{DS}		60	V
Gate-Source Voltage	V_{GS}		± 20	V
Continuous Drain Current	I_D	$T_C=25^\circ\text{C}$	57	A
		$T_C=100^\circ\text{C}$	40	A
Pulsed Drain Current	I_{DM}		157	A
Continuous Drain Current	I_D	$T_A=25^\circ\text{C}$	13	A
		$T_A=100^\circ\text{C}$	9	A
Avalanche Energy $L=0.3\text{mH}$	E_{AS}		54	mJ
Power Dissipation ⁽²⁾	P_D	$T_C=25^\circ\text{C}$	56	W
		$T_C=100^\circ\text{C}$	28	W
Power Dissipation ⁽¹⁾	P_D	$T_A=25^\circ\text{C}$	3.1	W
		$T_A=100^\circ\text{C}$	1.6	W
Operating Junction Temperature	T_J		-55 to 175	$^\circ\text{C}$
Storage Temperature Range	T_{STG}		-55 to 175	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

Single Operation					
Parameter		Symbol	Typical	Maximum	Unit
Junction-to-Ambient Thermal Resistance ⁽¹⁾	Steady State	$R_{\theta JA}$	40	48	°C/W
Junction-to-Case Thermal Resistance ⁽²⁾	Steady State	$R_{\theta JC}$	1.9	2.7	

ELECTRONICS CHARACTERISTICS

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V$, $I_D = -250\mu A$	60			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	BV_{DSS}/T_J			29.5		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=60V$, $V_{GS}=0V$, $T_J=25^\circ C$			10	μA
		$V_{DS}=60V$, $V_{GS}=0V$, $T_J=125^\circ C$			250	μA
Gate-to-source Leakage Current	I_{GSS}	$V_{DS}=0V$, $V_{GS}=20V$			100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS}=V_{DS}$, $I_D=250\mu A$	1.3	1.7	2.1	V
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			-4.7		mV/°C
Drain-to-source On-resistance ⁽⁴⁾	$R_{DS(on)}$	$V_{GS}=10V$, $I_D=25A$		6.8	8.5	m Ω
		$V_{GS}=4.5V$, $I_D=25A$		10.5	13.3	
CHARGES, CAPACITANCES AND GATE RESISTANCE						
Input Capacitance	C_{ISS}	$V_{GS}=0V$, $f=1.0MHz$, $V_{DS}=25V$		1200		pF
Output Capacitance	C_{OSS}			535		
Reverse Transfer Capacitance	C_{RSS}			54		
Total Gate Charge ⁽⁵⁾	$Q_{G(TOT)}$	$V_{GS}=10V$, $V_{DS}=48V$, $I_D=25A$		21.6		nC

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Total Gate Charge ⁽⁵⁾	$Q_{G(TOT)}$	$V_{GS}=4.5V,$ $V_{DS}=48V, I_D=25A$		11.7		
Gate-to-Source Charge ⁽⁵⁾	Q_{GS}	$V_{GS}=10V,$ $V_{DS}=48V, I_D=25A$		2.9		
Gate-to-Drain Charge ⁽⁵⁾	Q_{GD}			5.9		
Gate Resistance	R_g	$f = 1MHz$		1.3		Ω
SWITCHING CHARACTERISTICS ⁽⁵⁾						
Turn-On Delay Time	$t_d(ON)$	$V_{GS}=4.5V,$ $V_{DS}=48V,$ $I_D=25A, R_G=1.0\Omega$		6.6		ns
Rise Time	t_r			37.8		
Turn-Off Delay Time	$t_d(OFF)$			16		
Fall Time	t_f			15.6		
Body Diode Reverse Recovery Time	t_{rr}	$I_F=25A,$ $dI/dt=100A/\mu s$		22.3		ns
Body Diode Reverse Recovery Charge	Q_{rr}	$I_F=25A,$ $dI/dt=100A/\mu s$		12.7		nC
BODY DIODE CHARACTERISTICS						
Forward Voltage ⁽⁴⁾	V_{SD}	$V_{GS}=0V, I_S=25A$	0.5	0.85	1.2	V

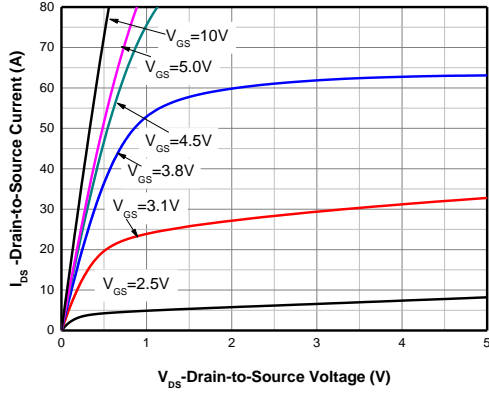
($T_J=25^\circ C$, unless otherwise noted.)

Note:

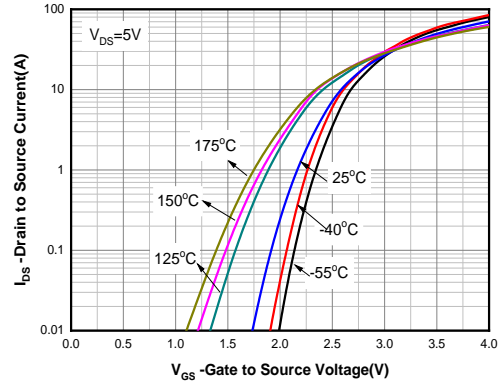
- (1) FR-4 board (38mm × 38mm × t1.6mm, 70 μ m Copper) partially covered with copper (645mm² area). The power dissipation P_{DSM} is based on Junction-to-Ambient thermal resistance value and the $T_{J(MAX)}=175^\circ C$. The value is only for reference, any application depends on the user's specific board design.
- (2) The power dissipation P_D is based on $T_{J(MAX)}=175^\circ C$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.
- (3) Repetitive rating, pulsed, duty cycle ~1%, keep initial $T_J=25^\circ C$, the maximum allowed junction temperature of 175 $^\circ C$.
- (4) The static characteristics are obtained using ~380 μs pulses, duty cycle ~1%.
- (5) The parameter is not subject to production test – verified by design / characterization.

TYPICAL CHARACTERISTICS

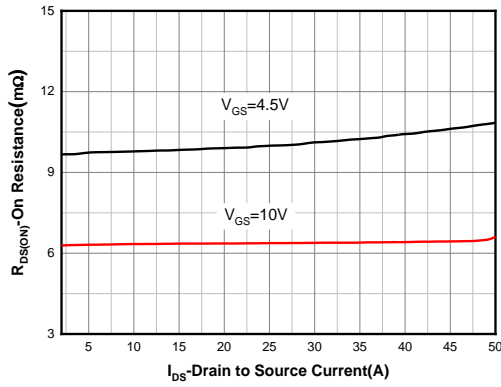
Ta=25°C, unless otherwise noted.



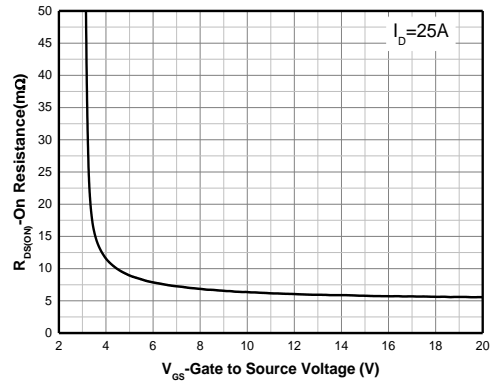
Output Characteristics ⁽⁴⁾



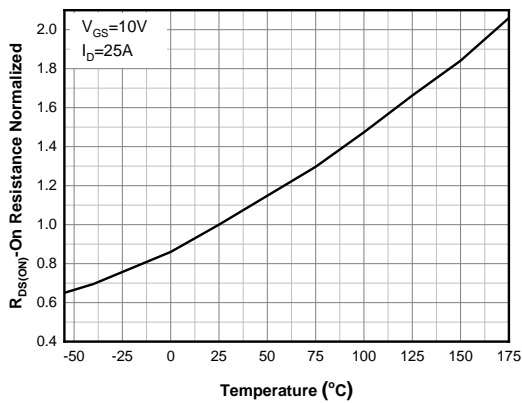
Transfer Characteristics ⁽⁴⁾



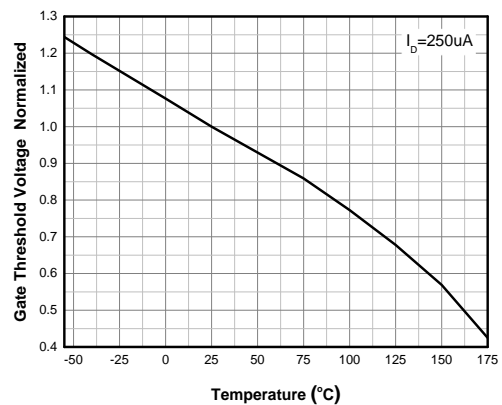
On-Resistance vs. Drain Current ⁽⁴⁾



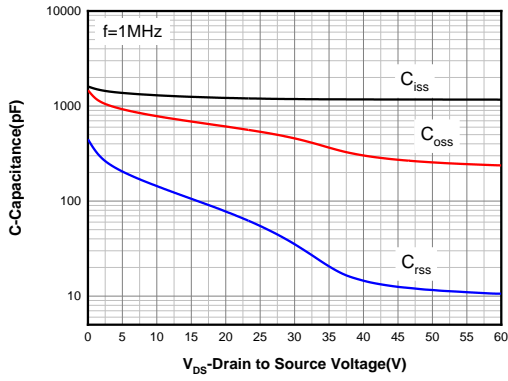
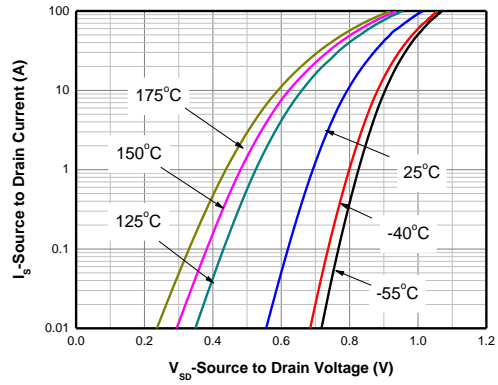
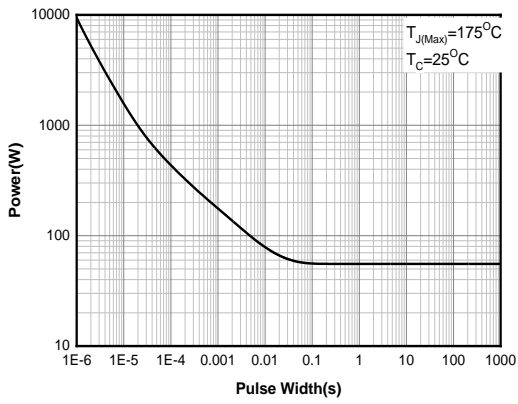
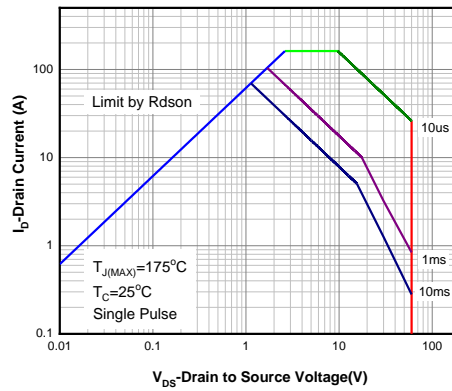
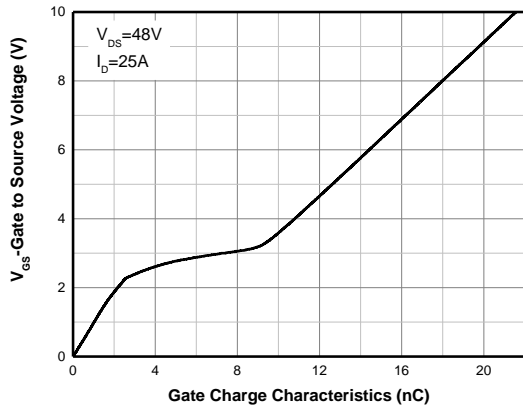
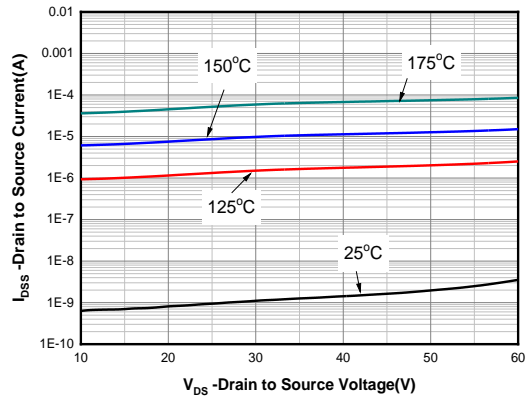
On-Resistance vs. Gate-to-Source Voltage ⁽⁴⁾

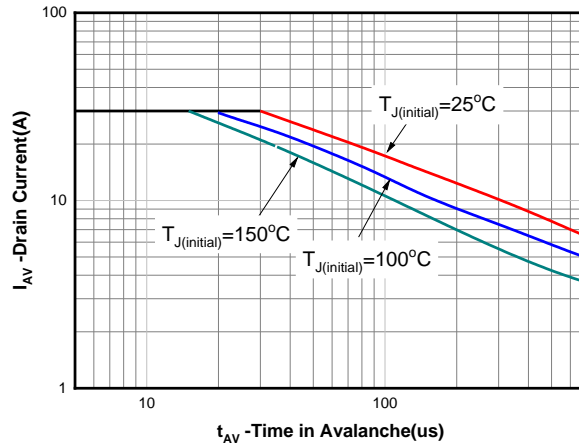
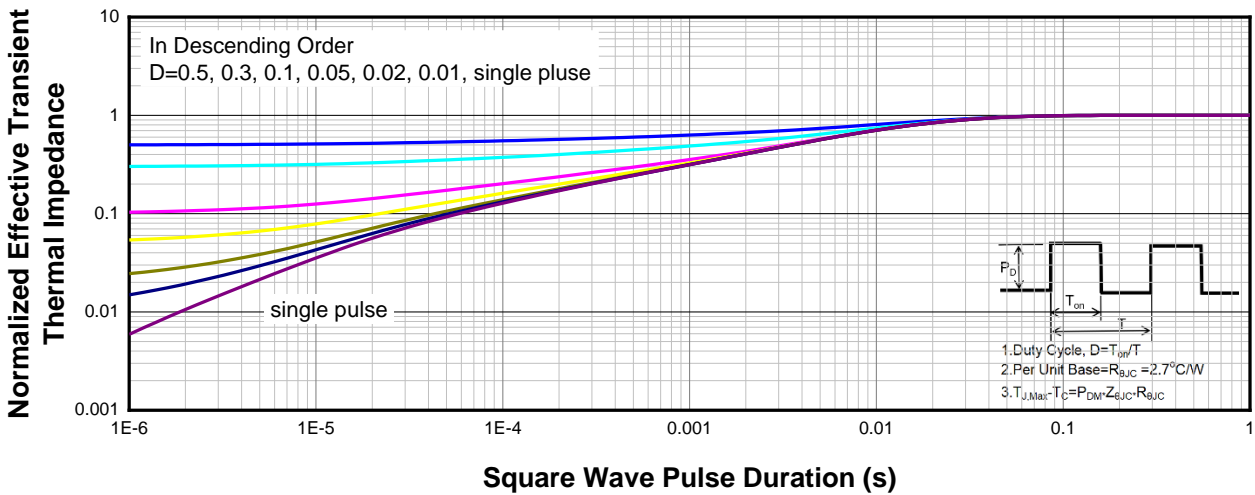
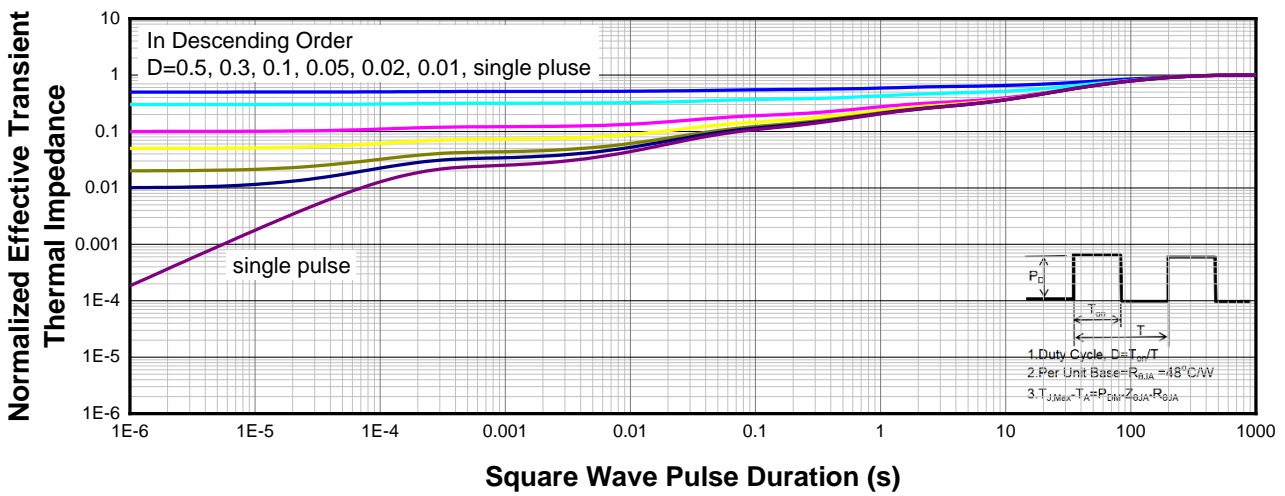


On-Resistance vs. Junction Temperature ⁽⁴⁾



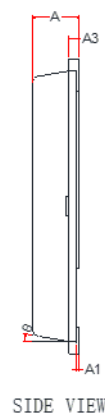
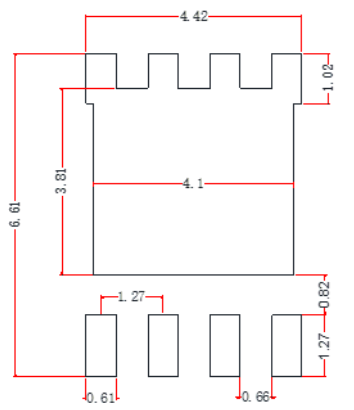
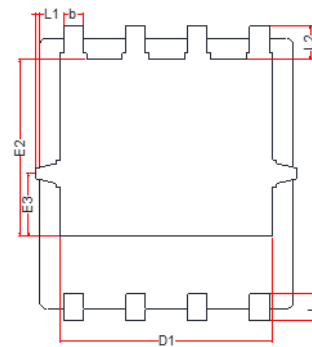
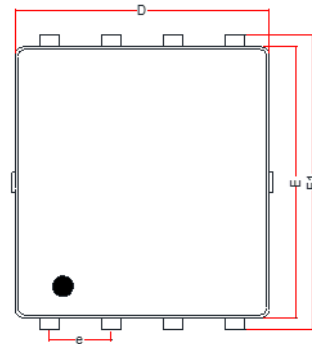
Threshold Voltage vs. Temperature

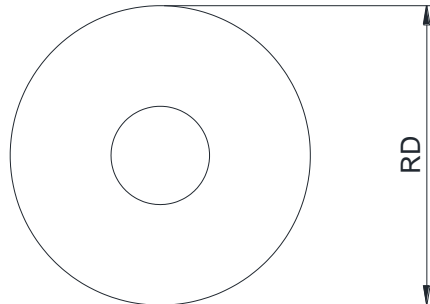
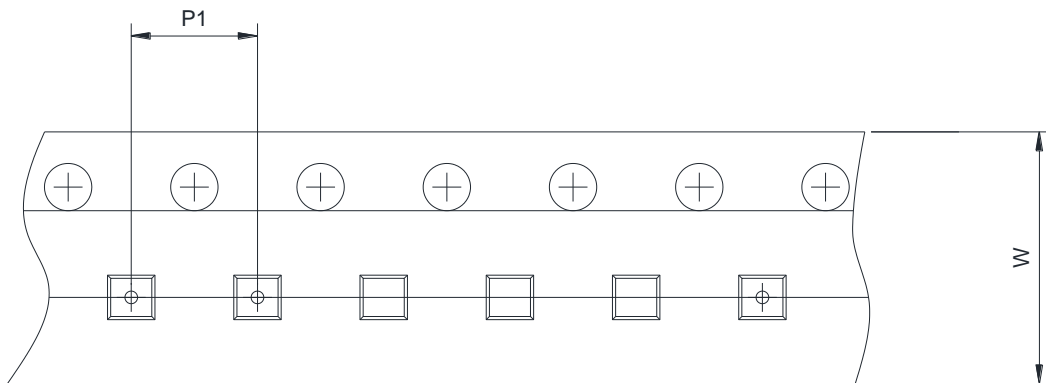
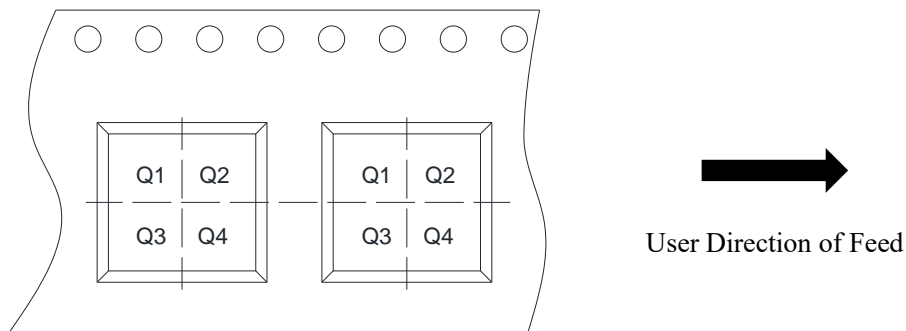

Capacitance

Body Diode Forward Voltage (4)

Single Pulse power

Safe Operating Area

Gate Charge Characteristics

Drain Current vs. Drain Voltage


Avalanche characteristics

Transient Thermal Response (Junction-to-Case)

Transient Thermal Response (Junction-to-Ambient)

PDFN5×6-8L DIMENSIONS
PACKAGE SIZE

Symbol	Min.	Typ.	Max.
A	0.85	0.95	1.00
A1	0.00	-	0.05
A3	-	0.2 Ref	-
b	0.30	0.40	0.50
D	5.10	5.20	5.30
E	5.45	5.55	5.65
e	1.27 BSC		
D1	4.25	4.35	4.45
E1	5.95	6.05	6.15
E2	3.525	3.625	3.725
E3	1.175	1.275	1.375
L	0.45	0.55	0.65
L1	0	-	0.15
L2	0.68 Ref		
θ	0 °	-	10 °



TAPE AND REEL INFORMATION
Reel Dimensions

Tape Dimensions

Quadrant Assignments For PIN1 Orientation In Tape


RD	Reel Dimension	<input type="checkbox"/> 7inch	<input checked="" type="checkbox"/> 13inch
W	Overall width of the carrier tape	<input type="checkbox"/> 8mm	<input checked="" type="checkbox"/> 12mm <input type="checkbox"/> 16mm
P1	Pitch between successive cavity centers	<input type="checkbox"/> 2mm	<input type="checkbox"/> 4mm <input checked="" type="checkbox"/> 8mm
Pin1	Pin1 Quadrant	<input checked="" type="checkbox"/> Q1	<input type="checkbox"/> Q2 <input type="checkbox"/> Q3 <input type="checkbox"/> Q4

ORDERING INFORMATION

TYPE NUMBER	PACKAGE	PACKING
SNM067R9DNAQ-8/TR	PDFN5×6-8L	Tape and reel

PDFN5×6-8L is packed with 5000 pieces/disc in braided packaging.

Important statement

SIT reserves the right to change the above-mentioned information without prior notice.

REVISION HISTORY

Version number	Datasheet status	Revision date
V1.0	Initial version.	May 2024