## FEATURES

- Compliant with LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A and SAE J260
- AEC-Q100 qualified
- Compatible with K line
- Integrated over-temperature protection function (thermal shutdown)
- Integrated bus pull-up slave termination resistor
- Bus current limiting protection
- Supply undervoltage protection
- Very low power consumption sleep mode and standby mode
- Support remote wake-up
- Support logic input levels with 3.3V and 5V
- LIN data transmission rate up to 20kbps
- Low ElectroMagnetic Emissions (EME)
- Available in SOP8 and DFN3*3-8 packages

## PRODUCT APPEARANCE

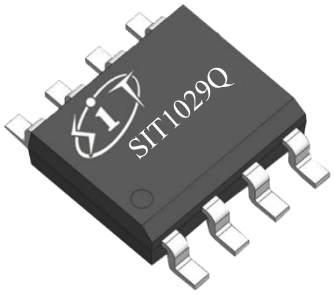



Fig 1. Provide environmentally friendly lead-free package

## DESCRIPTION

SIT1029Q is a local interconnect network (LIN) physical layer transceiver that complies with LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A, ISO 17987-4:2016 (12V) and SAE J2602 standards. It is mainly suitable for in-vehicle networks with a transmission rate of 1kbps to 20kbps. SIT1029Q controls the state of the LIN bus through the TXD pin, and can convert the data stream sent by the protocol controller into a bus signal with the best slew rate and waveform shaping to minimize electromagnetic radiation emission (EME). The LIN bus output pin has an internal pull-up resistor. Only when used as a master node, the LIN bus port needs to be pulled up to $V_{BAT}$ through an external resistor in series with a diode. SIT1029Q receives the data stream on the bus through the LIN pin, and transmits the data to the external microcontroller through the receiver's output pin RXD.

SIT1029Q can operate from 5.5V to 18V and support 12V applications. SIT1029Q has an extremely low quiescent current consumption in sleep mode and standby mode. It can quickly minimize power consumption in the event of a failure. The device can be placed in normal mode via a signal on the pin SLP_N. SIT1029Q supports integrated TXD dominant timeout detection function.

## PIN CONFIGURATION

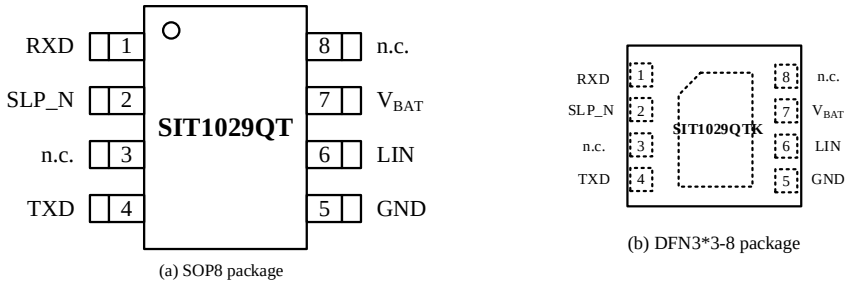



Fig 2. SIT1029Q pin configuration diagrams

## PIN DESCRIPTION

Table 1. SIT1029Q pin description

| Pin | Symbol | Description |
|---|---|---|
| 1 | RXD | receive data output (open-drain); active LOW after a wake-up event |
| 2 | SLP_N | sleep control input (active LOW); resets wake-up request on RXD |
| 3 | n.c. | not connected |
| 4 | TXD | transmit data input |
| 5 | GND | ground |
| 6 | LIN | LIN bus line input/output |
| 7 | $V_{BAT}$ | battery supply voltage |
| 8 | n.c. | not connected |

NOTE: In the DFN3*3-8 package, the pad on the back is connected to the GND pin of the chip. In order to obtain better heat dissipation performance, the pad on the back can be connected to a suitable “ground” on the PCB board.

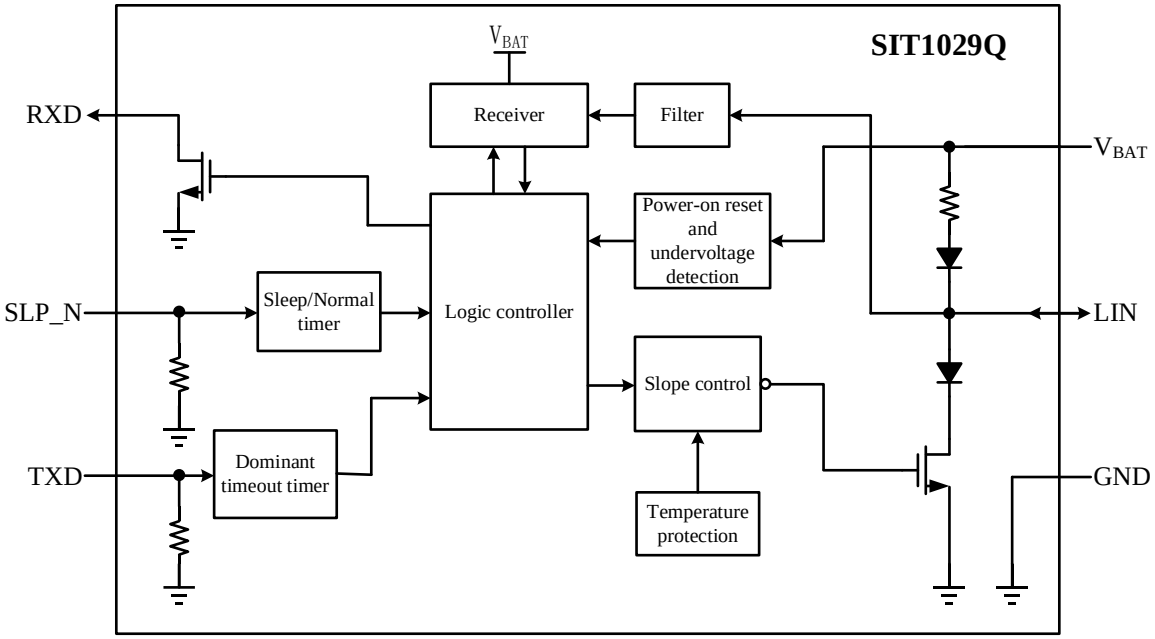



Fig 3. Block diagram

# FEATURE DESCRIPTION

## 1 Overview

The SIT1029Q is an interface device used between the LIN protocol controller and the physical bus. It can be used for in-vehicle and industrial control with a data rate up to 20kBd. The SIT1029Q receives the data stream sent by protocol controller at the pin TXD, and converts it into a bus signal with appropriate slew rate and waveform shaping. The input data on LIN bus is output to external microcontroller by pin RXD. This device is compliant with LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A, ISO 17987-4:2016 (12V) and SAE J2602 standards.

## 2 Short-circuit protection

Pin TXD provides an internal pull-down to GND to apply a predefined level on TXD when it is not enabled. The pin SLP_N also provides an internal pull-down to force the transceiver to enter sleep mode when SLP_N is not enabled.

Pin RXD will be left floating and limit the output current of transmitter to prevent a short-circuit between transmitter and $V_{BAT}$ or GND if the supply on pin $V_{BAT}$ is turned off. The power outage (pin $V_{BAT}$ and GND) has no effect on the bus and microcontroller. The bus has no reverse current, and the LIN transceiver can be disconnected from the power supply without affecting the LIN bus.

## 3 Thermal Shutdown

In normal mode, the over-temperature protection circuit will disable the output driver when the junction temperature of SIT1029Q exceeds the shutdown junction temperature $T_{j(sd)}$. When the junction temperature is lower than the hysteresis temperature, the driver is enabled again.

## 4 Undervoltage detection on $V_{BAT}$

If $V_{BAT}$ is lower than $V_{th(VBATL)L}$ during use, the protection circuit will disable the output driver. When $V_{BAT}$> $V_{th(VBATL)H}$, the driver will be enabled again.

## 5 Operating modes

As shown in Fig 4, the SIT1029Q supports four functional modes for very-low-power operation (Sleep mode), standby operation (Standby mode), normal operation (Normal mode) and power-up (Power-on mode). The operating states in each mode are shown in Table 2.

**Sleep mode:** This mode is the most power saving mode of the SIT1029Q. It can be woken up remotely via pin LIN, or activated directly via pin SLP_N. In order to prevent SIT1029Q from waking up due to accidental wake-up events caused by automotive transients or EMI, filters are designed at the receiver's input (LIN pin) and SLP_N pin. The necessary condition for SIT1029Q to be awakened in sleep mode is: the time to wake it up remotely through the LIN pin must be greater than $t_{wake(dom)LIN}$ (the wake-up time of LIN); the time to wake up directly through the SLP_N pin must be greater than $t_{gotonorm}$.

In normal mode, when SLP_N pin has a falling edge and SLP_N remains low for longer than $t_{gotosleep}$, SIT1029Q enters sleep mode.

**Standby mode:** SIT1029Q has very low static power consumption in this mode. When SIT1029Q is in sleep mode, if a remote wake-up event is detected, the device will automatically enter standby mode immediately, and the low level on the RXD pin will indicate that the wake-up process is used to send an interrupt flag to the MCU.

Setting pin SLP_N high during Standby mode may result in the following events:

(1) A change into Normal mode if the high level on pin SLP_N has been maintained for a certain time period ($t_{gotonorm}$).

(2) An immediate reset of the wake-up request signal on pin RXD.

**Normal mode:** Only in Normal mode, the receiver and transmitter are active and the SIT1029Q is able to transmit and receive data via the LIN bus. The high level of bus represents recessive and low level represents dominant. The receiver detects the data stream on the LIN bus and outputs it to the microcontroller via pin RXD. Normal mode is entered as a high level on pin SLP_N and maintained for a time of at least $t_{gotonorm}$ while the SIT1029Q is in Sleep or Standby mode. The Sleep mode is entered by setting pin SLP_N low for longer than $t_{gotosleep}$.

**Power-on mode:** If the voltage on $V_{BAT}$ is less than the low-level reset threshold $V_{th(VBATL)L}$ when powering on, the SIT1029Q is in power-on reset mode and all input and output functions are disabled; when the voltage on $V_{BAT}$ is greater than the high-level reset threshold $V_{th(VBAT)H}$, SIT1029Q enters sleep mode.

## 6 Wake Up Events

In sleep mode, the device can be awakened by the following two ways:

(1) Remote wake-up via pin LIN;

(2) Wake up directly via mode transition. If SLP_N is held HIGH for $t_{gotonorm}$, the device will switch from sleep mode to normal mode.

## 7 Remote Wake Up Events

LIN pin remote wake-up: When the LIN pin is pulled down to a low level through a falling edge, a rising edge appears at the next moment, and the low-level holds time between the rising edge and the falling edge at the previous moment is greater than $t_{wake(dom)LIN}$, the process is regarded as effective remote wake-up (as shown in Fig 5).

After the remote wake-up, the wake-up request event interrupts the microcontroller with the low level of the RXD pin as the indicator signal.

## 8 Dominant Timeout Function

If the TXD pin is forced to be permanently low due to hardware and/or software application failures, the integrated TXD dominant timeout timer circuit prevents the bus line from being driven to a permanently dominant state (blocking all network communications). The timer is triggered by the falling edge on the TXD pin. If the low level on the TXD pin holds longer than the internal timer time ($t_{to(dom)TXD}$), the transmitter will be disabled and the drive bus will go into a recessive state. The timer is reset by the rising edge on the TXD pin.

## 9 Failure Safety Feature

- The interior of the TXD pin is pulled down to the ground to prevent the undefined floating state of the TXD pin.
- The interior of the SLP_N pin is pulled down to the ground, and the corresponding LIN transceiver will enter the sleep mode when the SLP_N pin is floating.
- The ground loss condition has no effect on the bus port, and the bus port has no reverse current.
- The bus driver output stage current limiting to prevent the driver from burning down or functional effects when the bus short-circuits to the $V_{BAT}$.
- To avoid the effects caused by TXD pins being forced to permanently low due to hardware and/or

software application failures, after switching to normal mode, the LIN driver will be enabled only if a high TXD level is detected.

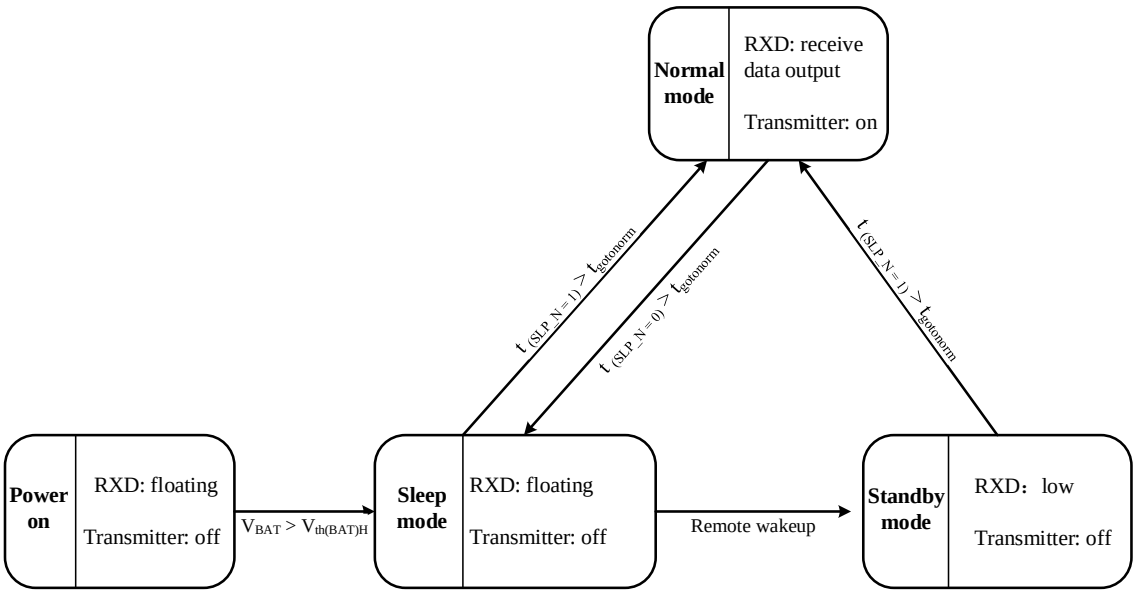



Fig 4. State diagram

Table 2. Working status of SIT1029Q in each mode

| Mode | SLP_N | RXD | Transmitter | Remarks |
|---|---|---|---|---|
| Sleep | low | floating | off | no wake-up request detected |
| Standby | low | low | off | wake-up request detected |
| Normal | high | recessive: high<br>dominant: low | on | Enable bus signal shaping |
| Power-on | low | floating | off | Disable all input and output functions |

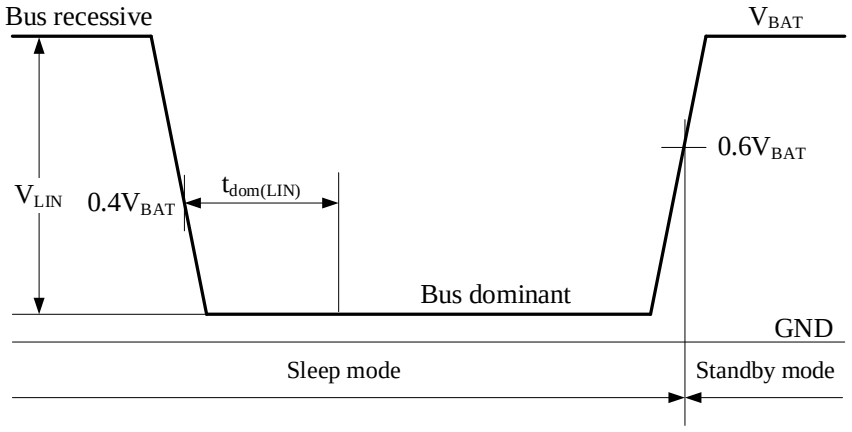



Fig 5. Remote wake-up behavior

## LIMITING VALUES

| Parameter | Symbol | Conditions | Range | Unit |
|---|---|---|---|---|
| battery supply voltage | $V_{BAT}$ | with respect to GND | -0.3 ~ +42 | V |
| voltage on pin TXD | $V_{TXD}$ | ISLP_N no limitation | -0.3 ~ +6 | V |
| | | $I_{SLP\_N}$ < 500μA | -0.3 ~ +7 | |
| voltage on pin RXD | $V_{RXD}$ | ISLP_N no limitation | -0.3 ~ +6 | V |
| | | $I_{SLP\_N}$ < 500μA | -0.3 ~ +7 | |
| voltage on pin SLP_N | $V_{SLP\_N}$ | ISLP_N no limitation | -0.3 ~ +6 | V |
| | | $I_{SLP\_N}$ < 500μA | -0.3 ~ +7 | |
| voltage on pin LIN | $V_{LIN}$ | with respect to GND | -42 ~ +42 | V |
| virtual junction temperature | $T_j$ | | -40 ~ 150 | °C |
| storage temperature | $T_{stg}$ | | -55 ~ 150 | °C |
| ambient temperature | $T_{amb}$ | | -40 ~ 125 | °C |
| ESD, human body model | $V_{ESD}$ | On pins LIN and VBAT | -8 ~ +8 | kV |
| | | On pins RXD, SLP_N and TXD | -2 ~ +2 | kV |
| ESD, charge device model | | All pins | -750 ~ +750 | V |
| ESD, machine model | | All pins | -200 ~ +200 | V |
| ESD, IEC61000-4-2 | | On pins LIN and VBAT | -4 ~ +4 | kV |

The maximum limit parameters mean that exceeding these values may cause irreversible damage to the device. Under these conditions, it is not conducive to the normal operation of the device. The continuous operation of the device at the maximum allowable rating may affect the reliability of the device. The reference point for all voltages is ground.

## STATIC CHARACTERISTICS

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Supply** | | | | | | |
| battery supply voltage | $V_{BAT}$ | | 5.5 | 12 | 18 | V |
| **Power consumption** | | | | | | |
| battery supply current | $I_{BAT}$ | Sleep mode bus recessive ($V_{LIN}$=$V_{BAT}$; $V_{SLP\_N}$=0V) | 1 | 4 | 10 | μA |
| | | Sleep mode bus dominant ($V_{LIN}$=$V_{BAT}$; $V_{SLP\_N}$=0V) | 100 | 350 | 1000 | μA |
| | | Standby mode bus recessive ($V_{LIN}$=$V_{BAT}$; $V_{SLP\_N}$=0V) | 1 | 4 | 10 | μA |
| | | Standby mode bus dominant ($V_{BAT}$=12V; $V_{LIN}$=0V; $V_{SLP\_N}$=0V) | 100 | 350 | 1000 | μA |
| | | Normal mode bus recessive ($V_{LIN}$=$V_{BAT}$; $V_{TXD}$=5V; $V_{SLP\_N}$=5V) | 50 | 160 | 300 | μA |
| | | Normal mode bus dominant ($V_{BAT}$=12V; $V_{TXD}$=0V; $V_{SLP\_N}$=5V) | 0.5 | 1.6 | 3 | mA |
| **Power-on reset** | | | | | | |
| LOW-level $V_{BAT}$ reset threshold voltage | $V_{th(VBATL)L}$ | | 3.9 | 4.4 | 4.7 | V |
| HIGH-level $V_{BAT}$ reset threshold voltage | $V_{th(VBATL)H}$ | | 4.2 | 4.7 | 5.1 | V |

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{BAT}$ reset hysteresis voltage | $V_{hys(VBATL)}$ [1] | | 0.15 | 0.3 | 0.6 | V |
| **Pin TXD** | | | | | | |
| HIGH-level input voltage | $V_{IH}$ | | 2 | - | 7 | V |
| LOW-level input voltage | $V_{IL}$ | | -0.3 | - | 0.8 | V |
| hysteresis voltage | $V_{hys}$ [1] | | 50 | 200 | 400 | mV |
| pull-down resistance on pin TXD | $R_{PD(TXD)}$ | $V_{TXD}$=5V | 50 | 125 | 400 | kΩ |
| **Pin SLP_N** | | | | | | |
| HIGH-level input voltage | $V_{IH}$ | | 2 | - | 7 | V |
| LOW-level input voltage | $V_{IL}$ | | -0.3 | - | 0.8 | V |
| hysteresis voltage | $V_{hys}$ [1] | | 50 | 200 | 400 | mV |
| pull-down resistance on pin SLP_N | $R_{PD(SLP\_N)}$ | $V_{SLP\_N}$=5V | 100 | 250 | 650 | kΩ |
| **Pin RXD** | | | | | | |
| LOW-level output current | $I_{OL}$ | Normal mode; $V_{RXD}$=0.4V; $V_{LIN}$=0V | 2 | - | - | mA |
| HIGH-level leakage current | $I_{LH}$ | Normal mode; $V_{RXD}$=5V; $V_{LIN}$=$V_{BAT}$ | -5 | - | 5 | μA |
| **Pin LIN** | | | | | | |
| current limitation for driver dominant state | $I_{BUS\_LIM}$ | $V_{TXD}$=0V; $V_{LIN}$=$V_{BAT}$=18V | 40 | - | 100 | mA |
| receiver recessive input leakage current | $I_{BUS\_PAS\_rec}$ | $V_{TXD}$=5V; $V_{LIN}$=18V; $V_{BAT}$=5.5V | - | - | 10 | μA |
| receiver dominant input leakage current | $I_{BUS\_PAS\_dom}$ | Normal mode; $V_{TXD}$=5V; $V_{LIN}$=0V; $V_{BAT}$=12V | -600 | - | - | μA |
| loss-of-ground bus current | $I_{BUS\_NO\_GND}$ | $V_{BAT}$=18V; $V_{LIN}$=0V | -1000 | - | 10 | μA |

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| loss-of-battery bus current | $I_{BUS\_NO\_BAT}$ | $V_{BAT}$=0V; $V_{LIN}$=18V | - | - | 10 | μA |
| receiver dominant input voltage | $V_{th(dom)RX}$ | | - | - | $0.4V_{BAT}$ | V |
| receiver recessive input voltage | $V_{th(rec)RX}$ | | $0.6V_{BAT}$ | - | - | V |
| receiver center voltage | $V_{th(RX)cntr}$ | $V_{th(RX)\ cntr}$= ($V_{th(rec)RX}$+ $V_{th(dom)RX}$)/2 | $0.475V_{BAT}$ | $0.5V_{BAT}$ | $0.525V_{BAT}$ | V |
| receiver hysteresis threshold voltage | $V_{th(hys)RX}$ | $V_{th(hys)RX}$= $V_{th(rec)RX}$-$V_{th(dom)RX}$ | - | - | $0.175V_{BAT}$ | V |
| slave resistance | $R_{slave}$ | connected between pins LIN and $V_{BAT}$; $V_{LIN}$=0V; $V_{BAT}$=12V; $V_{TXD}$=$V_{SLP\_N}$=5V | 20 | 30 | 60 | kΩ |
| capacitance on pin LIN | $C_{LIN}$ [1] | | - | - | 20 | pF |
| dominant output voltage | $V_{o(dom)}$ | Normal mode; $V_{TXD}$=0V; $V_{BAT}$=7V | - | - | 1.4 | V |
| | | Normal mode; $V_{TXD}$=0V; $V_{BAT}$=18V | - | - | 2.0 | V |
| **Thermal shutdown** | | | | | | |
| shutdown junction temperature | $T_{j(sd)}$ [1] | | 150 | - | 200 | °C |

(Unless specified otherwise; 5.5V≤$V_{BAT}$≤18V, -40°C≤$T_j$≤150°C; typical in $V_{BAT}$=12V, $T_{amb}$=25°C.)

[1] Not tested in production; guaranteed by design.

## SWITCH CHARACTERISTICS

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Duty cycles** | | | | | | |
| duty cycle 1 | $\delta 1$ [1][2] | $V_{th(rec)(max)}$=0.744×$V_{BAT}$; $V_{th(dom)(max)}$=0.581×$V_{BAT}$; $t_{bit}$=50µs; $V_{BAT}$=7V ~ 18V, Fig 6 | 0.396 | - | - | |
| | | $V_{th(rec)(max)}$=0.76×$V_{BAT}$; $V_{th(dom)(max)}$=0.593×$V_{BAT}$; $t_{bit}$=50µs; $V_{BAT}$=5.5V ~ 7V, Fig 6 | 0.396 | - | - | |
| duty cycle 2 | $\delta 2$ [2][3] | $V_{th(rec)(min)}$=0.422×$V_{BAT}$; $V_{th(dom)(min)}$=0.284×$V_{BAT}$; $t_{bit}$=50µs; $V_{BAT}$=7.6V ~ 18V, Fig 6 | - | - | 0.581 | |
| | | $V_{th(rec)(min)}$=0.41×$V_{BAT}$; $V_{th(dom)(min)}$=0.275×$V_{BAT}$; $t_{bit}$=50µs; $V_{BAT}$=6.1V ~ 7.6V, Fig 6 | - | - | 0.581 | |
| duty cycle 3 | $\delta 3$ [1][2] | $V_{th(rec)(max)}$=0.778×$V_{BAT}$; $V_{th(dom)(max)}$=0.616×$V_{BAT}$; $t_{bit}$=96µs; $V_{BAT}$=7V ~ 18V, Fig 6 | 0.417 | - | - | |
| | | $V_{th(rec)(max)}$=0.797×$V_{BAT}$; $V_{th(dom)(max)}$=0.630×$V_{BAT}$; $t_{bit}$=96µs; $V_{BAT}$=5.5V ~ 7V, Fig 6 | 0.417 | - | - | |
| duty cycle 4 | $\delta 4$ [2][3] | $V_{th(rec)(min)}$=0.389×$V_{BAT}$; $V_{th(dom)(min)}$=0.251×$V_{BAT}$; $t_{bit}$=96µs; $V_{BAT}$=7.6V ~ 18V, Fig 6 | - | - | 0.590 | |
| | | $V_{th(rec)(min)}$=0.378×$V_{BAT}$; $V_{th(dom)(min)}$=0.242×$V_{BAT}$; $t_{bit}$=96µs; $V_{BAT}$=6.1V ~ 7.6V, Fig 6 | - | - | 0.590 | |
| **Timing characteristics** | | | | | | |
| receiver propagation delay | $t_{PD(RX)}$ [4] | | - | - | 6 | µs |
| receiver propagation delay symmetry | $t_{PD(RX)sym}$ [4] | | -2 | - | 2 | µs |

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| LIN dominant wake-up time | $t_{wake(dom)LIN}$ | Sleep mode | 30 | 80 | 150 | μs |
| go to normal time | $t_{gotonorm}$ | | 2 | 6 | 10 | μs |
| go to sleep time | $t_{gotosleep}$ | | 2 | 6 | 10 | μs |
| Dominant time-out time | $T_{to(dom)TXD}$ | | 6 | 12 | 50 | ms |

(Unless specified otherwise; 5.5V≤$V_{BAT}$≤18V, -40°C≤$T_j$≤150°C; typical in $V_{BAT}$=12V, $T_{amb}$=25°C.)

[1] $\delta 1, \delta 3 = \frac{t_{bus(rec)(\min)}}{2 \times t_{bit}}$;

[2] Bus load condition: (1) $C_L$=1nF, $R_L$=1kΩ; (2) $C_L$=6.8nF, $R_L$=660Ω; (3) $C_L$=10nF, $R_L$=500Ω;

[3] $\delta 2, \delta 4 = \frac{t_{bus(rec)(\max)}}{2 \times t_{bit}}$;

[4] Load condition pin RXD: $C_{RXD}$=20pF, $R_{RXD}$=2.4kΩ.

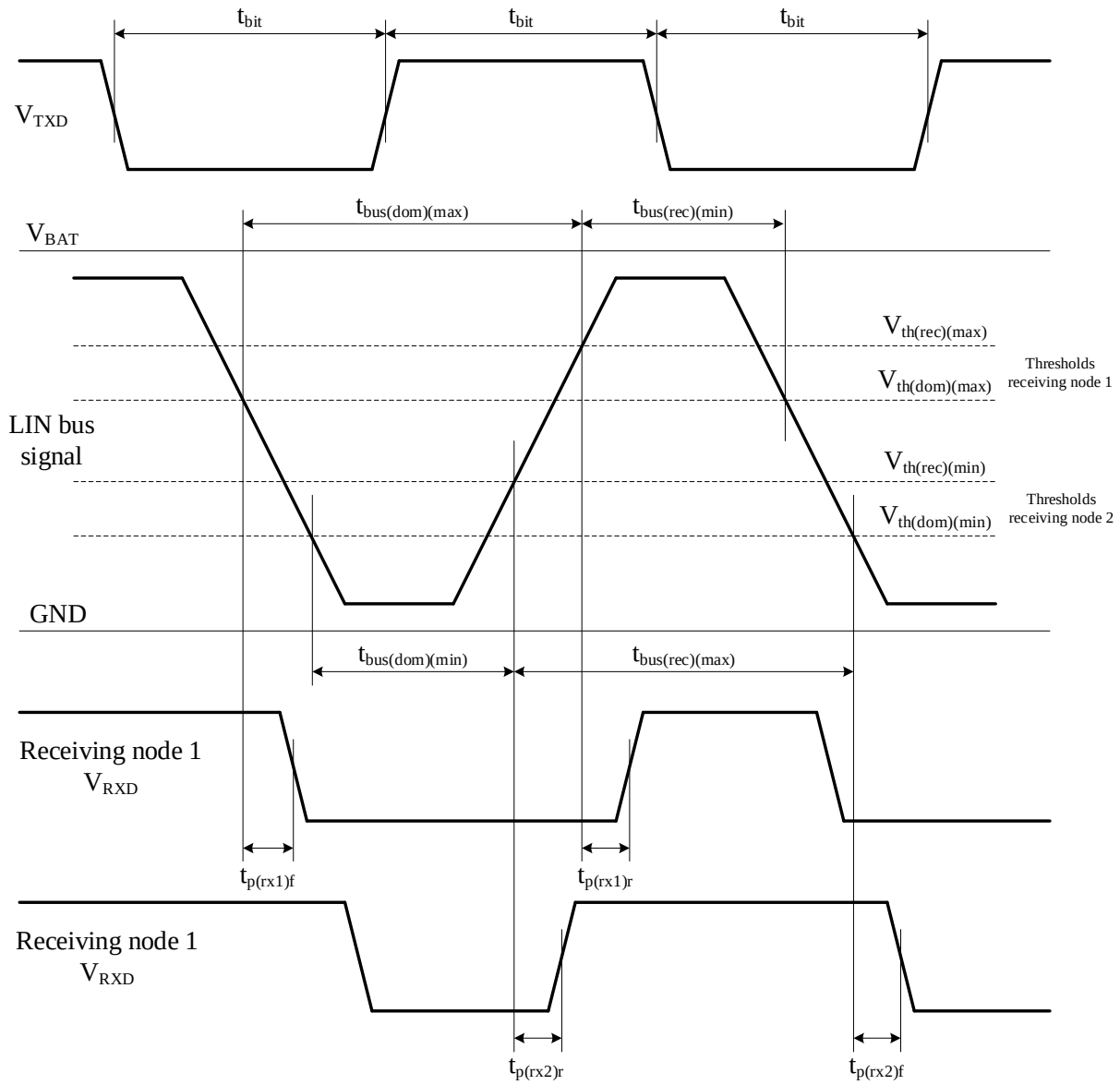



Fig 6. Bus signal transmission timing diagram

## TYPICAL APPLICATION

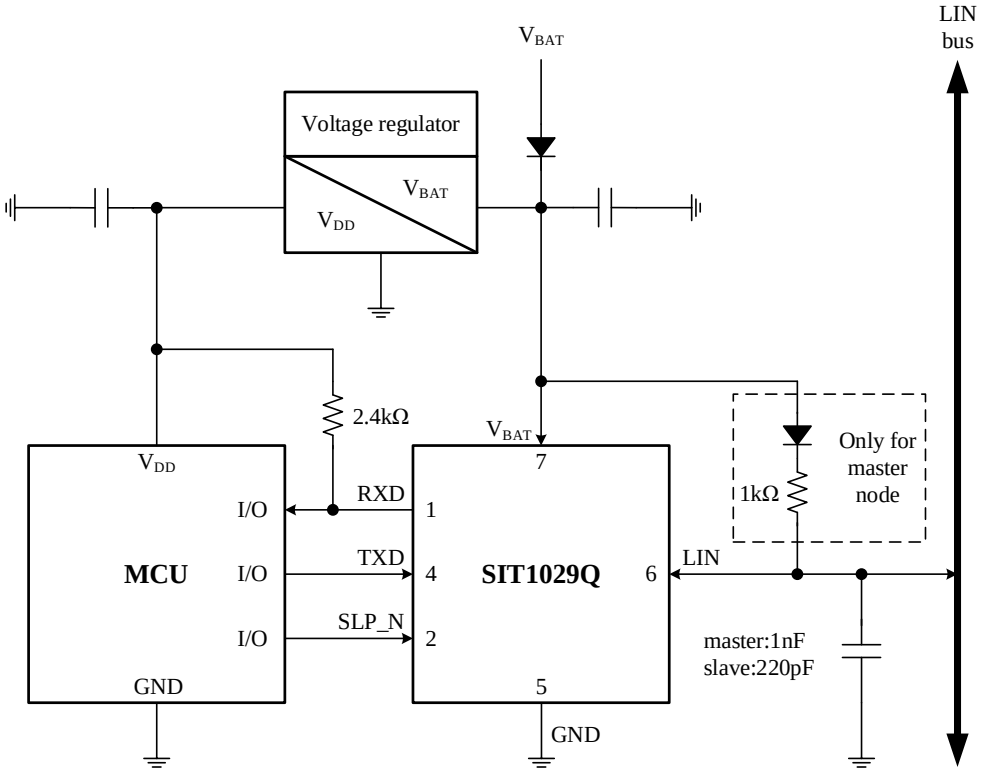



Fig 7. Typical application of the SIT1029Q

## TIMING TEST CIRCUIT

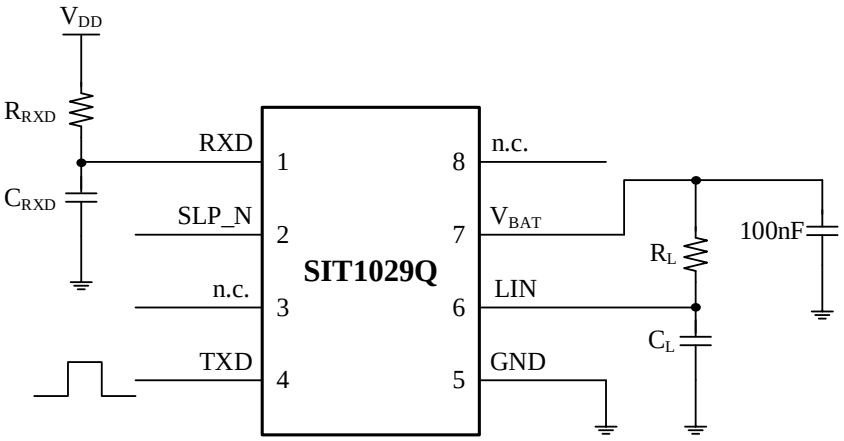
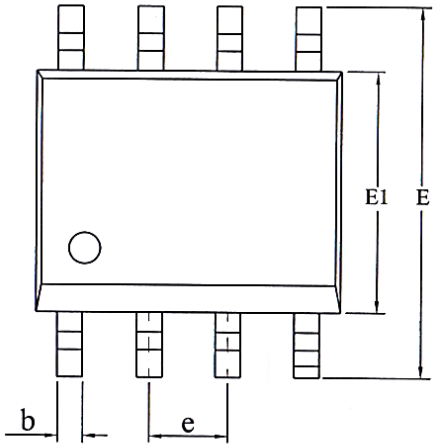


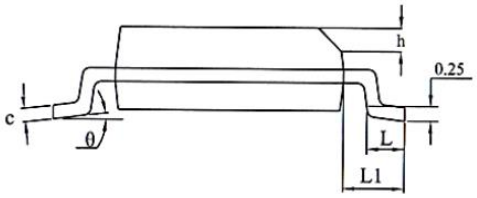

Fig 8. Timing test circuit

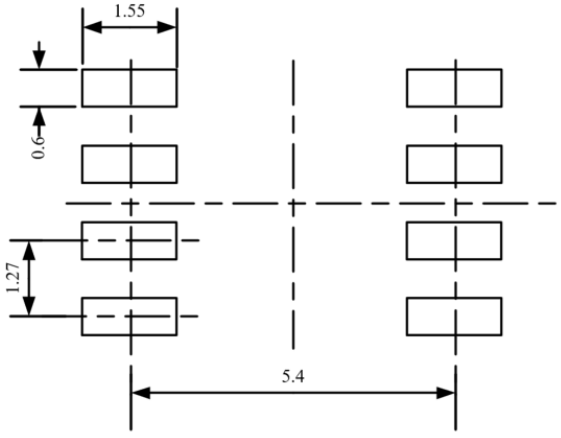
## SOP8 DIMENSIONS

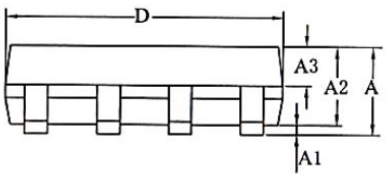
### PACKAGE SIZE

| SYMBOL | MIN./mm | TYP./mm | MAX./mm |
|---|---|---|---|
| A | 1.40 | - | 1.80 |
| A1 | 0.10 | - | 0.25 |
| A2 | 1.30 | 1.40 | 1.50 |
| A3 | 0.60 | 0.65 | 0.70 |
| b | 0.38 | - | 0.51 |
| D | 4.80 | 4.90 | 5.00 |
| E | 5.80 | 6.00 | 6.20 |
| E1 | 3.80 | 3.90 | 4.00 |
| e | 1.27BSC | | |
| L | 0.40 | 0.60 | 0.80 |
| L1 | 1.05REF | | |
| c | 0.20 | - | 0.25 |
| θ | 0° | - | 8° |



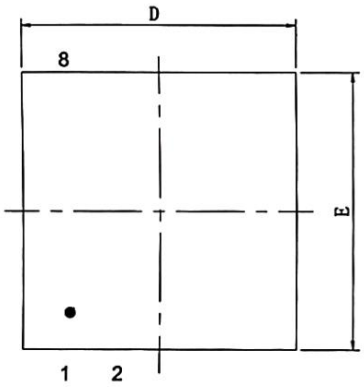



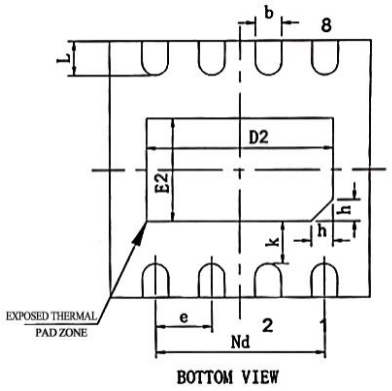

LAND PATTERN EXAMPLE (Unit: mm)

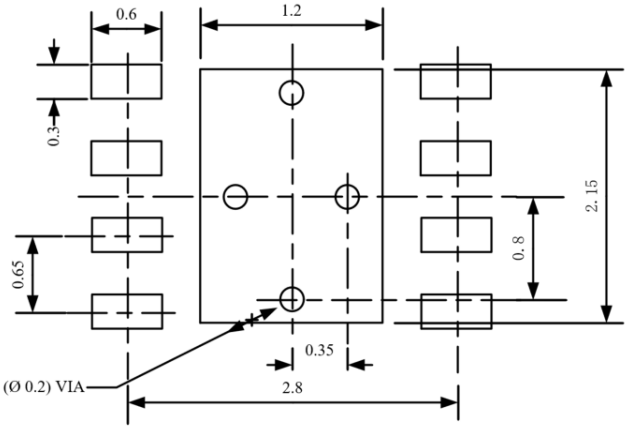
## DFN3*3-8 DIMENSIONS

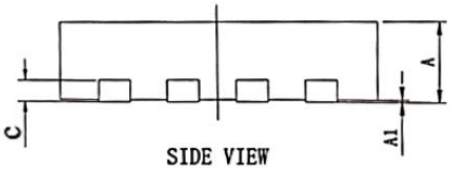
### PACKAGE SIZE

| SYMBOL | MIN/mm | TYP /mm | MAX/mm |
|---|---|---|---|
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0 | 0.02 | 0.05 |
| A3 | 0.203 REF | | |
| D | 2.90 | 3.00 | 3.10 |
| E | 2.90 | 3.00 | 3.10 |
| D2 | 2.05 | 2.15 | 2.25 |
| Nd | 1.95BSC | | |
| E2 | 1.10 | 1.20 | 1.30 |
| b | 0.25 | 0.30 | 0.35 |
| e | 0.65 TYP | | |
| k | 0.50REF | | |
| L | 0.35 | 0.4 | 0.45 |
| h | 0.20 | 0.25 | 0.30 |



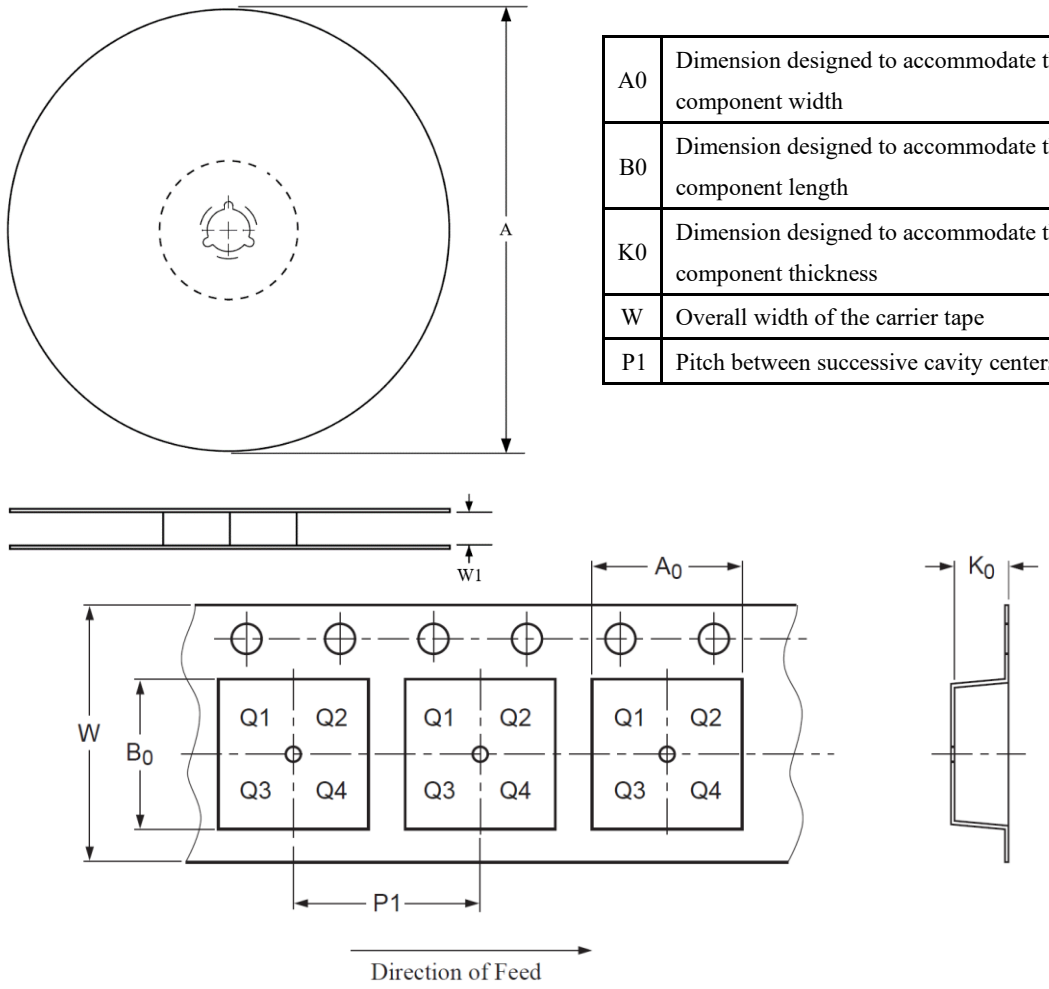




LAND PATTERN EXAMPLE (Unit: mm)

## TAPE AND REEL INFORMATION




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

PIN1 is in quadrant 1

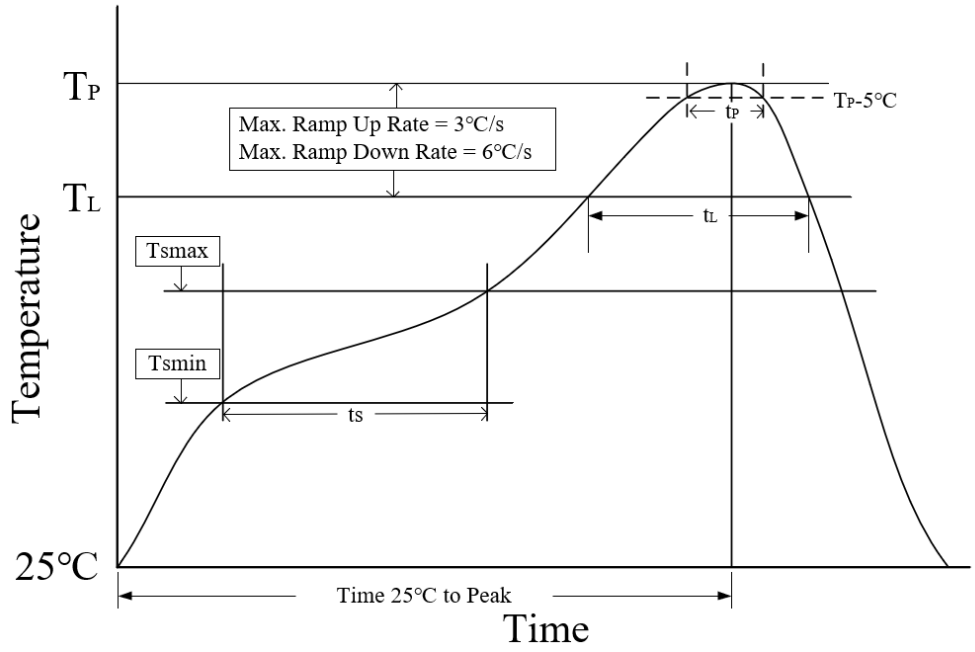
| Package type | Reel diameter A (mm) | Tape width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) |
|---|---|---|---|---|---|---|---|
| SOP8 | 330±1 | 12.4 | 6.60±0.1 | 5.30±0.10 | 1.90±0.1 | 8.00±0.1 | 12.00±0.1 |
| DFN3*3-8 | 329±1 | 12.4 | 3.30±0.1 | 3.30±0.1 | 1.10±0.1 | 8.00±0.1 | 12.00±0.3 |

## ORDERING INFORMATION

| TYPE NUMBER | PACKAGE | PACKING |
|---|---|---|
| SIT1029QT | SOP8 | Tape and reel |
| SIT1029QTK | DFN3*3-8, small outline package, no leads | Tape and reel |

SOP8 is packed with 2500 pieces/disc in braided packaging, with small outline package and 6000 pieces/disc in lead free packaging.

## REFLOW SOLDERING




| Parameter | Lead-free soldering conditions |
|---|---|
| Ave ramp up rate ($T_L$ to $T_P$) | 3 °C/second max |
| Preheat time ts ($T_{smin}$=150 °C to $T_{smax}$=200 °C) | 60-120 seconds |
| Melting time $t_L$ ($T_L$=217 °C） | 60-150 seconds |
| Peak temp $T_P$ | 260-265 °C |
| 5°C below peak temperature $t_P$ | 30 seconds |
| Ave cooling rate ($T_P$ to $T_L$) | 6 °C/second max |
| Normal temperature 25°C to peak temperature TP time | 8 minutes max |

**Important statement**

SIT reserves the right to change the above-mentioned information without prior notice.

## REVISION HISTORY

| Version number | Data sheet status | Revision date |
|---|---|---|
| V1.0 | Initial version. | September 2022 |
| V1.1 | Added ambient temperature $T_{amb;}$<br>Updated package dimension schematic (size unchanged). | March 2023 |
| V1.2 | Added “AEC-Q100 qualified”;<br>Added ESD related information. | September 2023 |