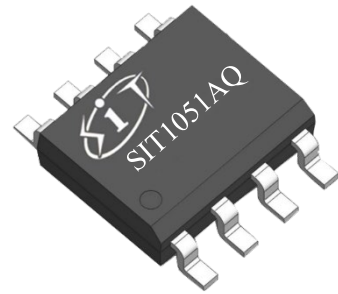


## FEATURES

- Fully compatible with the ISO 11898 standard
- AEC-Q100 qualified
- Thermally protected
- ±58V BUS protection
- Driver (TXD) dominant overtime function
- Silent receive mode
- SIT1051AQT/E with off mode in low power consumption
- SIT1051AQT/3 can be interfaced directly to microcontrollers with supply voltages from 3V to 5V
- Undervoltage protection on VCC and VIO power supply pins
- Timing guaranteed for data rates up to 5 Mbit/s in the (CAN FD) fast phase
- The typical loop delay from TXD to RXD is less than 100ns
- Very low ElectroMagnetic Emission (EME)
- Unpowered nodes do not interfere with the bus
- Provide DFN3\*3-8, small outline, leadless package

## PRODUCT APPEARANCE



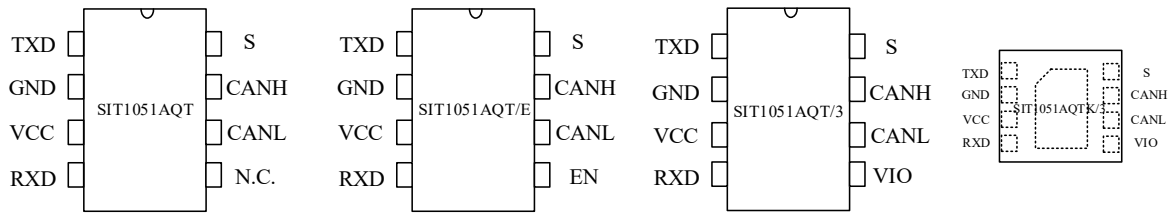
Provide Green and Environmentally  
 Friendly Lead-free package

## DESCRIPTION

SIT1051AQ is an interface chip used between the CAN protocol controller and the physical bus. It can be used for in-vehicle, industrial control and other fields. It supports 5Mbps (CAN FD), and has ability to perform differential signal transmission between bus and the CAN protocol controller.

The SIT1051AQ is an upgraded version of the SIT1051Q with improved bus signal symmetry and lower electromagnetic radiation performance. In addition, the SIT1051AQ is fully compatible with SIT1051Q.

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT
Supply voltage	VCC		4.5	5.5	V
Maximum transmission rate	1/t <sub>bit</sub>	Non-return to zero code	5		Mbaud
CANH/CANL input or output voltage	V <sub>can</sub>		-58	+58	V
Bus differential voltage	V <sub>diff</sub>		1.5	3.0	V
Virtual junction temperature	T <sub>j</sub>		-40	150	°C

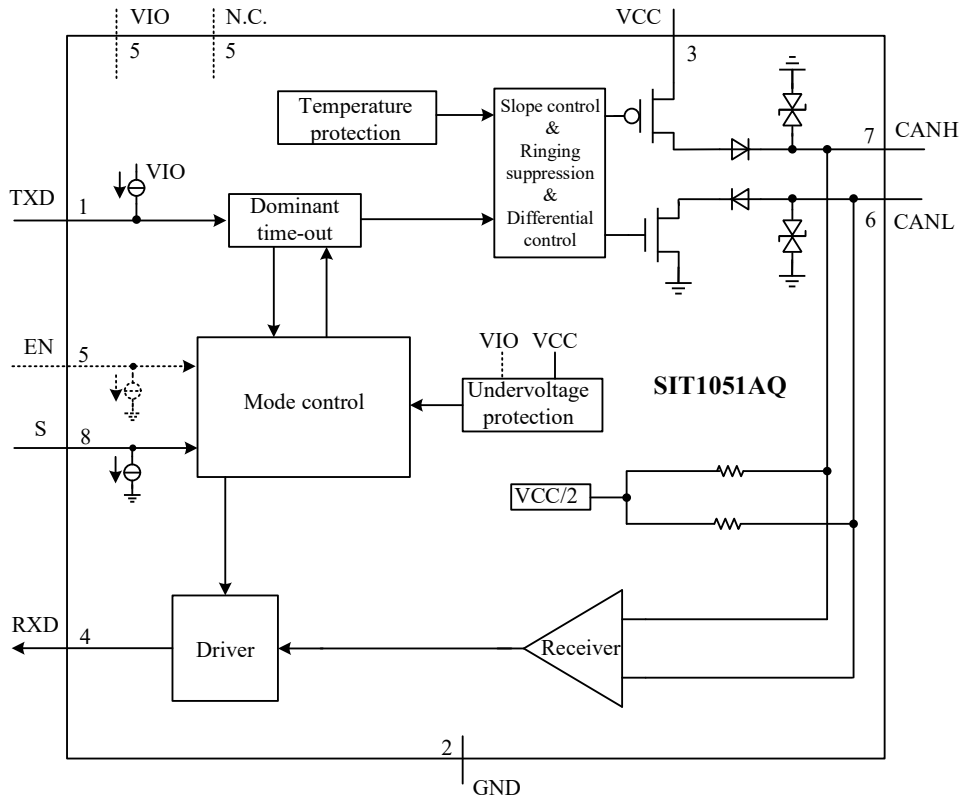
**PIN CONFIGURATION**

**PIN DESCRIPTION**

PIN	SYMBOL	DESCRIPTION
1	TXD	transmit data input
2	GND	ground
3	VCC	supply voltage
4	RXD	receive data output; reads out data from the bus lines
5	N.C.	no connection (SIT1051AQT version)
5	VIO	transceiver I/O level conversion power supply voltage (SIT1051AQT/3 version)
5	EN	off mode enable pin. The low level is the off mode (SIT1051AQT/E version)
6	CANL	LOW-level CAN-bus line
7	CANH	HIGH-level CAN-bus line
8	S	silent mode control input, low level is high speed mode

**LIMITING VALUES**

PARAMETER	SYMBOL	VALUE	UNIT
Supply voltage	VCC	-0.3~7	V
MCU side port	TXD, RXD, S, EN, VIO	-0.3~7	V
Bus side input voltage	CANL, CANH	-58~58	V
Bus differential breakdown voltage	$V_{CANH-CANL}$	-27~27	V
Storage temperature	$T_{stg}$	-55~150	°C
Virtual junction temperature	$T_j$	-40~150	°C
Welding temperature range		300	°C

The maximum limit parameters mean that exceeding these values may cause irreversible damage to the device. Under these conditions, it is not conducive to the normal operation of the device. The continuous operation of the device at the maximum allowable rating may affect the reliability of the device. The reference point for all voltages is ground.

**INTERNAL CIRCUIT BLOCK DIAGRAM**


**DRIVER ELECTRICAL CHARACTERISTICS**

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
CANH dominant output voltage	$V_{OH(D)}$	Normal mode, TXD=0V, $R_L=50\Omega$ to $65\Omega$	2.75	3.5	4.5	V
CANL dominant output voltage	$V_{OL(D)}$		0.5	1.5	2.25	V
Bus dominant differential output voltage	$V_{OD(D)}$	Normal mode, TXD=0V, $R_L=50\Omega$ to $65\Omega$	1.5		3	V
		Normal mode, TXD=0V, $R_L=45\Omega$ to $70\Omega$	1.4		3.3	V
		Normal mode, TXD=0V, $R_L=2240\Omega$	1.5		5	V
Bus recessive output voltage	$V_{O(R)}$	Normal mode, TXD=VIO, No load	2	0.5V <sub>CC</sub>	3	V
Bus recessive differential output voltage	$V_{OD(R)}$	Normal mode, TXD=VIO, No load	-500		50	mV
Transmitter dominant voltage symmetry	$V_{dom(TX)sym}$	$V_{dom(TX)sym}=V_{CC}-$ CANH - CANL	-400		400	mV
Transmitter voltage symmetry	$V_{TXsym}$	$V_{TXsym}= CANH +$ CANL, $R_L=60\Omega$ , $C_{SPLIT}=4.7nF$ , $f_{TXD}=250kHz$ , 1MHz, 2MHz <a href="#">Fig 5</a>		0.9V <sub>CC</sub>	1.1V <sub>CC</sub>	V
Dominant-recessive common-mode output voltage difference	$V_{cm(step)}$	<a href="#">Fig 3</a> , <a href="#">Fig 5</a>	-150		150	mV
Dominant-recessive common-mode peak-to-peak	$V_{cm(p-p)}$	<a href="#">Fig 3</a> , <a href="#">Fig 5</a>	-300		300	mV
Dominant short-circuit output current	$I_{O(SC)DOM}$	Normal mode, TXD=0V, CANH= -15V to 40V	-100	-70	-40	mA

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Dominant short-circuit output current	$I_{O(SC)DOM}$	Normal mode, TXD=0V, CANL=-15V to 40V	40	70	100	mA
Recessive short-circuit output current	$I_{O(SC)REC}$	Normal mode, TXD=VIO, CANH=CANL=-27V to 32V	-3		3	mA

Unless otherwise stated, all typical values are measured at 25°C, supply voltage VCC=5V, VIO=5V (if applicable), RL=60Ω.

## DRIVER SWITCHING CHARACTERISTICS

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation delay time, low-to-high level output	$t_{d(TXD-busdom)}$	Normal mode, <a href="#">Fig 1</a> , <a href="#">Fig 4</a>		45		ns
Propagation delay time, high-to-low level output	$t_{d(TXD-busrec)}$	Normal mode, <a href="#">Fig 1</a> , <a href="#">Fig 4</a>		55		ns
Differential output signal rise time	$t_{r(BUS)}$			45		ns
Differential output signal fall time	$t_{f(BUS)}$			45		ns

Unless otherwise stated, all typical values are measured at 25°C, supply voltage VCC=5V, VIO=5V (if applicable), RL=60Ω.

## RECEIVER ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Receiver threshold voltage	$V_{th(RX)dif}$	Normal mode and silent mode, $-30V < V_{CM} < 30V$	0.5		0.9	V
Receiver threshold voltage hysteresis range	$V_{hys(RX)dif}$	Normal mode and silent mode, $-30V < V_{CM} < 30V$	50	120	400	mV
Receiver recessive voltage range	$V_{rec(RX)}$	Normal mode and silent mode, $-30V < V_{CM} < 30V$	-3		0.5	V
Receiver dominant voltage range	$V_{dom(RX)}$	Normal mode and silent mode, $-30V < V_{CM} < 30V$	0.9		8	V

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Bus leakage current	$I_L$	VCC=VIO=0V, CANH= CANL=5V	-10		10	$\mu$ A
CANH, CANL input resistance	$R_{IN}$	$-2V \leq CANH \leq 7V$ $-2V \leq CANL \leq 7V$	9	15	28	k $\Omega$
CANH, CANL differential-input resistance	$R_{ID}$	$-2V \leq CANH \leq 7V$ $-2V \leq CANL \leq 7V$	19	30	52	k $\Omega$
CANH, CANL input resistance mismatch	$\Delta R_{IN}$	$0V \leq CANH \leq 5V$ $0V \leq CANL \leq 5V$	-2		2	%
CANH, CANL input capacitance to ground	$C_{IN}$	TXD=VIO		24		pF
CANH, CANL differential-input capacitance	$C_{ID}$	TXD=VIO		12		pF
Bus slew rate	SR	Bus differential voltage dominant to recessive edge			70	V/ $\mu$ s

Unless otherwise stated, all typical values are measured at 25°C, supply voltage VCC=5V, VIO=5V (if applicable), RL=60 $\Omega$ .

## RECEIVER SWITCHING CHARACTERISTICS

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation delay time, low-to-high level output	$t_{d(busdom-RXD)}$	Normal mode <a href="#">Fig 1</a> , <a href="#">Fig 4</a>		45		ns
Propagation delay time, low-to-high level output	$t_{d(busrec-RXD)}$	Normal mode <a href="#">Fig 1</a> , <a href="#">Fig 4</a>		45		ns
RXD signal rise time	$t_{r(RXD)}$			8		ns
RXD signal fall time	$t_{f(RXD)}$			8		ns

Unless otherwise stated, all typical values are measured at 25°C, supply voltage VCC=5V, VIO=5V (if applicable), RL=60 $\Omega$ .

**DEVICE SWITCHING CHARACTERISTIC**

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Loop delay 1, TXD falling edge to RXD falling edge	$t_{loop1}$	Normal mode <a href="#">Fig 1</a> , <a href="#">Fig 4</a>	40		160	ns
Loop delay 2, TXD rising edge to RXD rising edge	$t_{loop2}$	Normal mode <a href="#">Fig 1</a> , <a href="#">Fig 4</a>	40		175	ns
Bit time of BUS output pin	$t_{bit(BUS)}$	$t_{bit(TXD)}=500ns$	435		530	ns
		$t_{bit(TXD)}=200ns$	155		210	ns
Bit time of RXD output pin	$t_{bit(RXD)}$	$t_{bit(TXD)}=500ns$	400		550	ns
		$t_{bit(TXD)}=200ns$	120		220	ns
Time difference between BUS and RXD output bits	$\Delta t_{rec}$	$\Delta t_{rec}=t_{bit(RXD)}-t_{bit(BUS)}$ ; $t_{bit(TXD)}=500ns$	-65		40	ns
		$\Delta t_{rec}=t_{bit(RXD)}-t_{bit(BUS)}$ ; $t_{bit(TXD)}=200ns$	-45		15	ns
TXD dominant timeout	$t_{dom\_TXD}$		0.8	2	4	ms

Unless otherwise stated, all typical values are measured at 25°C, supply voltage VCC=5V, VIO=5V (if applicable), RL=60Ω.

**TXD PIN CHARACTERISTICS**

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
HIGH-level input current	$I_{IH}(TXD)$	TXD=VIO	-5		5	μA
LOW-level input current	$I_{IL}(TXD)$	TXD=0V	-260	-150	-30	μA
Leakage current of TXD without power	$I_{O(off)}$	VCC=VIO=0V, TXD=5.5V	-1		1	μA
HIGH-level input voltage	$V_{IH}$	SIT1051AQT/3	0.7VIO <sup>(1)</sup>		VIO+0.3	V
LOW-level input voltage	$V_{IL}$	SIT1051AQT/3	-0.3		0.3VIO	V
HIGH-level input voltage	$V_{IH}$	SIT1051AQT	2		VCC+0.3	V
LOW-level input voltage	$V_{IL}$	SIT1051AQT	-0.3		0.8	V

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Open voltage on TXD pin	TXD <sub>O</sub>			H		logic

(1) SIT1051QT/E version, VIO=VCC;

Unless otherwise stated, all typical values are measured at 25°C, supply voltage VCC=5V, VIO=5V (if applicable), R<sub>L</sub>=60Ω.

## S PIN CHARACTERISTICS

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
HIGH-level input current	I <sub>IH</sub> (S)	S=VIO	1		10	μA
LOW-level input current	I <sub>IL</sub> (S)	S=0V	-1		1	μA
Leakage current of S without power	I <sub>O</sub> (off)	VCC=VIO=0V, S=5.5V	-1		1	μA
HIGH-level input voltage	V <sub>IH</sub>	SIT1051AQT/3	0.7VIO <sup>(1)</sup>		VIO+0.3	V
LOW-level input voltage	V <sub>IL</sub>	SIT1051AQT/3	-0.3		0.3VIO	V
HIGH-level input voltage	V <sub>IH</sub>	SIT1051AQT	2		VCC+0.3	V
LOW-level input voltage	V <sub>IL</sub>	SIT1051AQT	-0.3		0.8	V
Open voltage on S pin	S <sub>O</sub>			L		logic

(1) SIT1051QT/E version, VIO=VCC;

Unless otherwise stated, all typical values are measured at 25°C, supply voltage VCC=5V, VIO=5V (if applicable), R<sub>L</sub>=60Ω.

## EN PIN

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
HIGH-level input current	I <sub>IH</sub> (EN)	EN=VCC	1		10	μA
LOW-level input current	I <sub>IL</sub> (EN)	EN=0V	-1		1	μA
HIGH-level input voltage	V <sub>IH</sub>		0.7VCC		VCC+0.3	V
LOW-level input voltage	V <sub>IL</sub>		-0.3		0.3VCC	V



PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Leakage current of EN without power	$I_{O(off)}$	VCC=0V EN=5.5V	-1		1	$\mu A$
Open voltage on EN pin	EN <sub>O</sub>		L			logic

Unless otherwise stated, all typical values are measured at 25°C, supply voltage VCC=5V, VIO=5V (if applicable), R<sub>L</sub>=60Ω.

## RXD PIN CHARACTERISTICS

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
HIGH-level input current	$I_{OH(RXD)}$	VIO=VCC, RXD=VIO-0.4V	-8	-3	-1	mA
LOW-level input current	$I_{OL(RXD)}$	RXD=0.4V, Bus dominant	2	5	12	mA
Leakage current of RXD without power	$I_{O(off)}$	VCC=VIO=0V, RXD=5.5V	-1		1	$\mu A$

Unless otherwise stated, all typical values are measured at 25°C, supply voltage VCC=5V, VIO=5V (if applicable), R<sub>L</sub>=60Ω.

## SUPPLY CURRENT

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
VCC supply current	$I_{CC\_D}$	Normal mode dominant		45	70	mA
	$I_{CC\_R}$	Normal mode recessive		5	10	mA
	$I_{CC\_S}$	Silent mode		1.5	3	mA
	$I_{CC\_OFF}$	Off mode (SIT1051AQT/E)		5	8	$\mu A$
VIO supply current	$I_{IO\_D}$	TXD=0V		170	300	$\mu A$
	$I_{IO\_R}$	TXD=VIO		15	30	$\mu A$

Unless otherwise stated, all typical values are measured at 25°C, supply voltage VCC=5V, VIO=5V (if applicable), R<sub>L</sub>=60Ω.

### OVERTEMPERATURE PROTECTION

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Shutdown junction temperature	$T_{j(sd)}$			190		°C

Unless otherwise stated, all typical values are measured at 25°C, supply voltage VCC=5V, VIO=5V (if applicable),  $R_L=60\Omega$ .

### UNDERVOLTAGE PROTECTION

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
VCC undervoltage protection	$V_{uvd\_VCC}$		3.7	4	4.3	V
VIO undervoltage protection	$V_{uvd\_VIO}$		1.7	2	2.3	V

Unless otherwise stated, all typical values are measured at 25°C, supply voltage VCC=5V, VIO=5V (if applicable),  $R_L=60\Omega$ .

### ESD PERFORMANCE

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
CAN bus pin contact discharge model (IEC)	$V_{ESD\_IEC}$	IEC 61000-4-2: Contact discharge (CANH, CANL)	-4		+4	kV
Human body model (HBM)	$V_{ESD\_HBM}$	All ports	-8		+8	kV
Charged device model (CDM)	$V_{ESD\_CDM}$		-750		+750	V
Machine model (MM)	$V_{ESD\_MM}$		-300		+300	V

**FUNCTION TABLE**
**Table1. CAN TRANSCEIVER TRUTH TABLE**

TXD <sup>(1)</sup>	S <sup>(1)</sup>	CANH <sup>(1)</sup>	CANL <sup>(1)</sup>	BUS STATE	RXD <sup>(1)</sup>
L	L or open	H	L	Dominate	L
H or open	L	0.5VCC	0.5VCC	Recessive	H
X	H	0.5VCC	0.5VCC	Recessive	H

(1) H=high level; L=low level; X=irrelevant.

**Table 2. RECEIVER FUNCTION TABLE**

V <sub>ID</sub> =CANH-CANL	BUS STATE	RXD <sup>(1)</sup>
V <sub>ID</sub> ≥0.9V	Dominate	L
0.5<V <sub>ID</sub> <0.9V	?	?
V <sub>ID</sub> ≤0.5V	Recessive	H

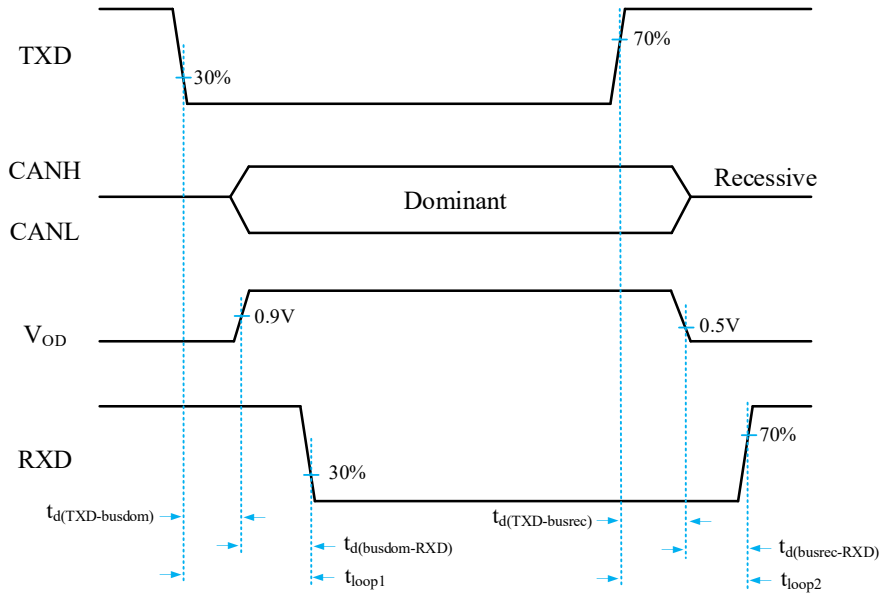
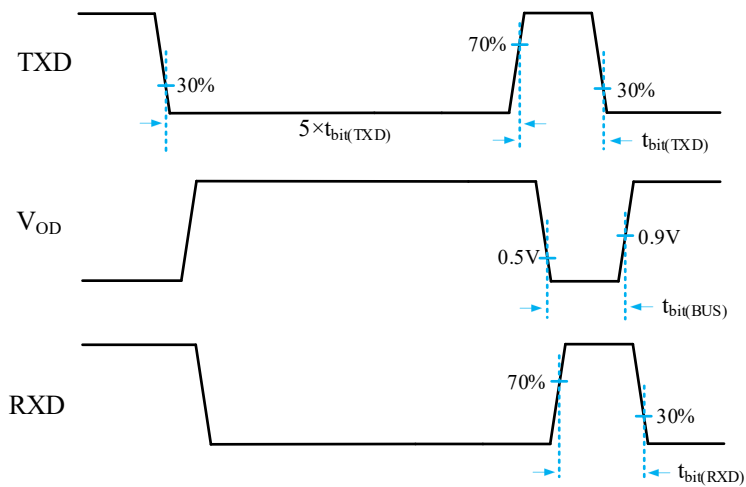
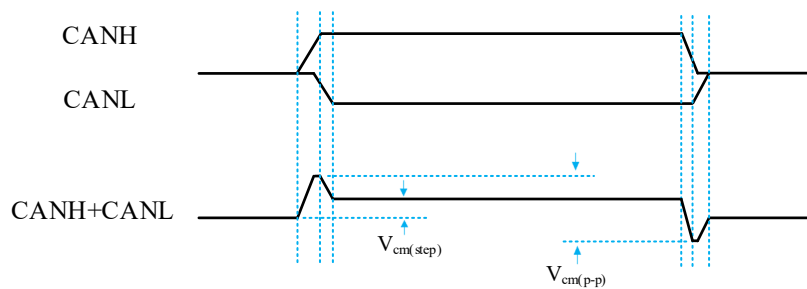
(1) H= high level; L= low level; ?= uncertain.

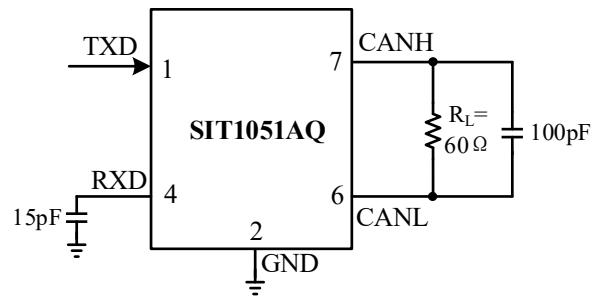
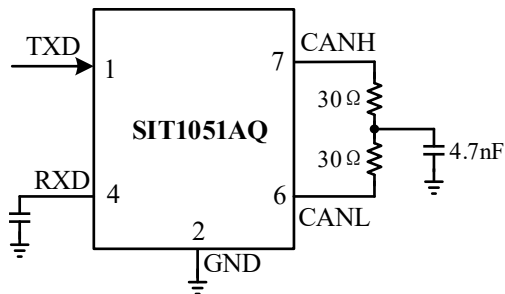
**Table 3. UNDERVOLTAGE PROTECTION STATUS TABLE**

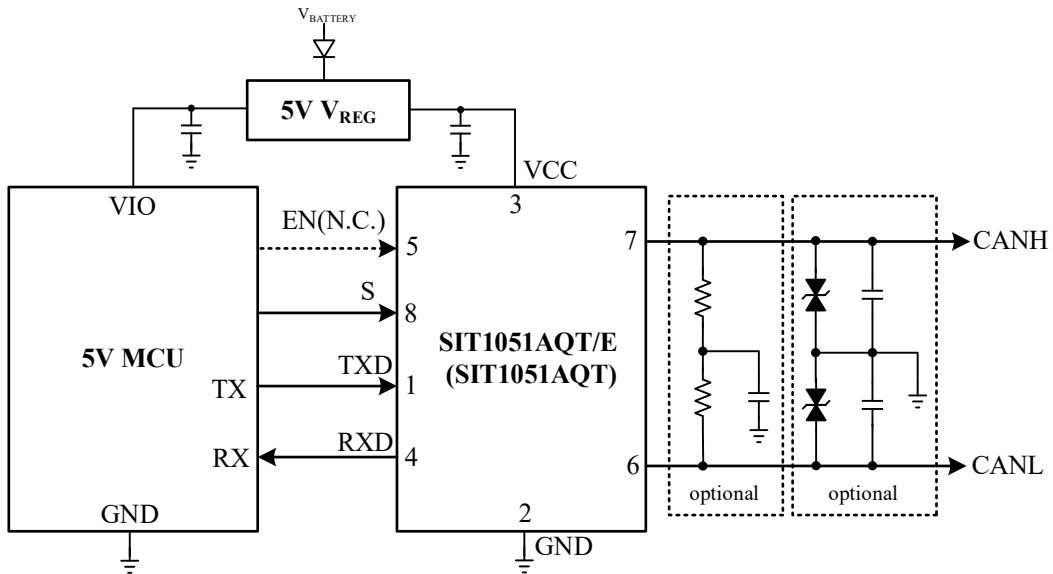
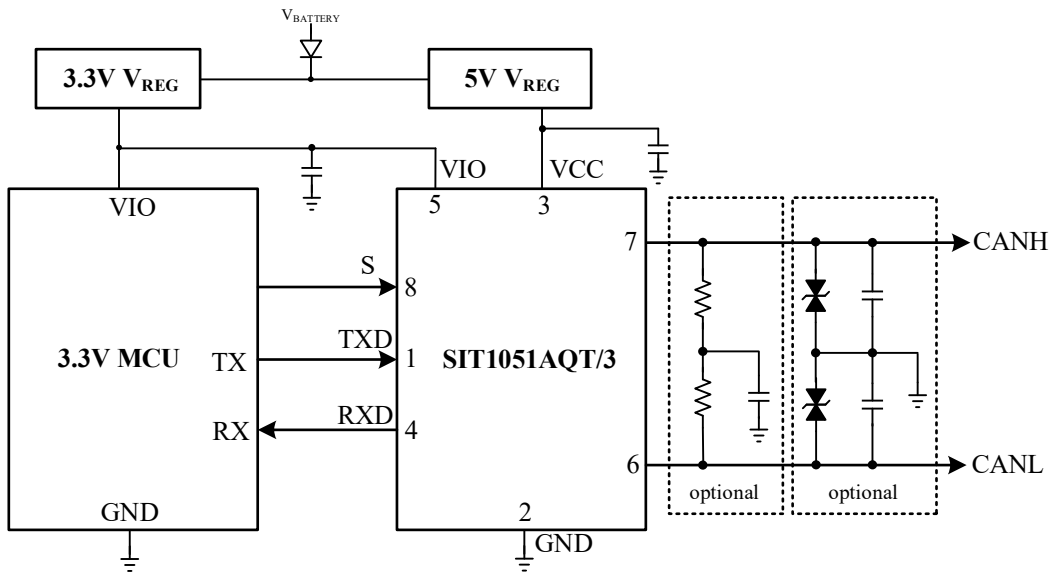
VCC	VIO <sup>(1)</sup>	BUS STATE	BUS OUTPUT <sup>(2)</sup>	RXD <sup>(2)</sup>
VCC>V <sub>uvd_VCC</sub>	VIO>V <sub>uvd_VIO</sub>	Normal	According to S and TXD	Follow the bus
VCC<V <sub>uvd_VCC</sub>	VIO>V <sub>uvd_VIO</sub>	Protected status	Z	H
VCC>V <sub>uvd_VCC</sub>	VIO<V <sub>uvd_VIO</sub>	Protected status	Z	H
VCC<V <sub>uvd_VCC</sub>	VIO<V <sub>uvd_VIO</sub>	Protected status	Z	H

(1) SIT1051AQT/3 and SIT1051AQTK/3 version;

(2) H=high level; Z=high ohmic.

**TIMING WAVEFORM**

**Fig 1 Transceiver transmission delay**

**Fig 2  $t_{bit}$  delay**

**Fig 3 Bus common-mode voltage (SAE 1939-14)**

**TEST**

**Fig 4 Transceiver timing sequence test circuit**

**Fig 5 Transceiver bus symmetry test circuit**

**TYPICAL APPLICATION DIAGRAM**

**Fig 6 SIT1051AQT/E (or SIT1051AQT) and 5V MCU typical application diagram**

**Fig 7 SIT1051AQT/3 and 3.3V MCU typical application diagram**

## ADDITIONAL DESCRIPTION

### 1 Sketch

SIT1051AQ is an interface chip applied between the CAN protocol controller and the physical bus. It can be used for in-vehicle, industrial control and other fields. It supports 5Mbps flexible data rate (CAN FD) and has ability to transmit differential signals between the bus and the CAN protocol controller. Fully compatible with ISO 11898 standard.

### 2 Short-circuit protection

A current-limiting circuit protects the transmitter output stage from damage caused by accidental short-circuit to either positive or negative supply voltage, although power dissipation increases during this fault condition.

### 3 Overtemperature protection

SIT1051AQ has an overtemperature protection function. When the overtemperature protection is triggered, the current of the driver stage will be reduced. Because the driver tube is the main energy consuming component, the current reduction will reduce the power consumption and thus reduce the chip temperature. Meanwhile, the rest of the chip still works.

### 4 Undervoltage protection

The SIT1051AQ power pin has an undervoltage detection function to place the device in protected mode, which can protect the bus (bus output high ohmic state) when VCC is below  $V_{\text{uvd\_VCC}}$  or VIO is below  $V_{\text{uvd\_VIO}}$  (if applicable).

### 5 Control mode

The control pin S allows two modes of operation to be selected: high speed mode and silent mode.

The high-speed mode is the normal operating mode and is optional by grounding pin S or floating it. CAN driver and the receiver can work completely normally and CAN communication is bidirectional.

Set pin S to high level to activate silent mode. The CAN driver will shut off and the receiver will continue working.

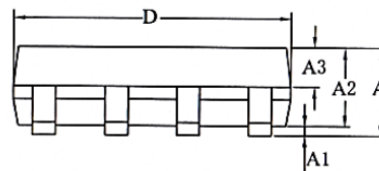
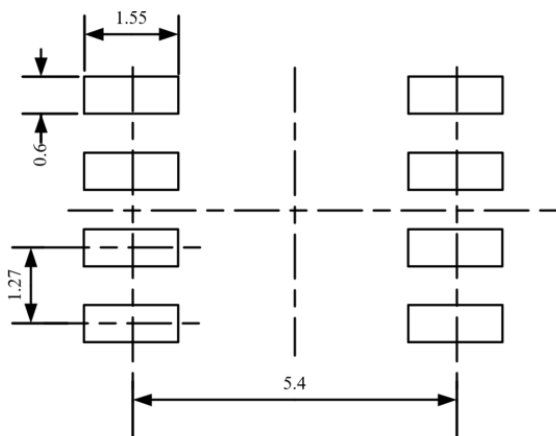
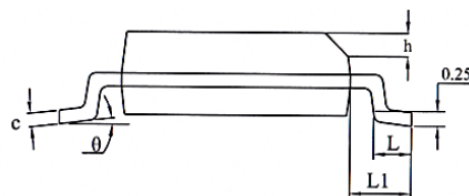
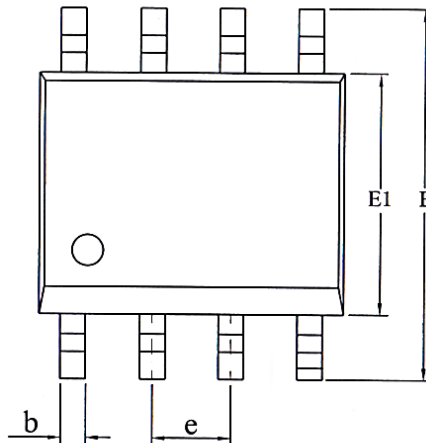
### 6 TXD dominant time-out function

A 'TXD dominant time-out' timer circuit prevents the bus lines from being driven to a permanent dominant state (blocking all network communication) if pin TXD is forced permanently LOW by a hardware and/or software application failure. The timer is triggered by a negative edge on pin TXD.

If the duration of the LOW level on pin TXD exceeds the internal timer value ( $t_{\text{dom}}$ ), the transmitter is disabled, driving the bus lines into a recessive state. The timer is reset by a positive edge on pin TXD.

**SOP8 DIMENSIONS**
**PACKAGE SIZE**

SYMBOL	MIN./mm	TYP./mm	MAX./mm
A	1.40	-	1.80
A1	0.10	-	0.25
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.38	-	0.51
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
L	0.40	0.60	0.80
L1	1.05REF		
c	0.20	-	0.25
$\theta$	0°	-	8°

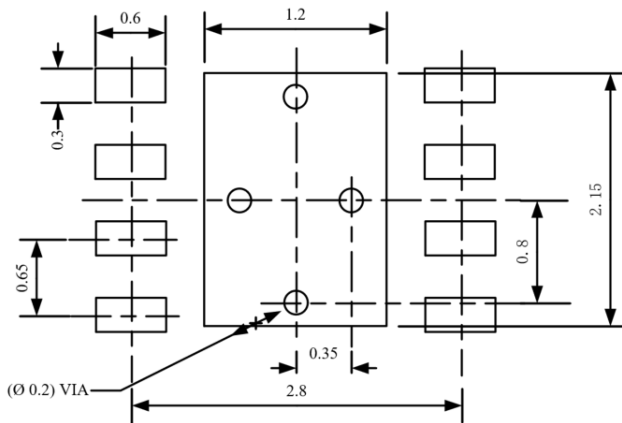
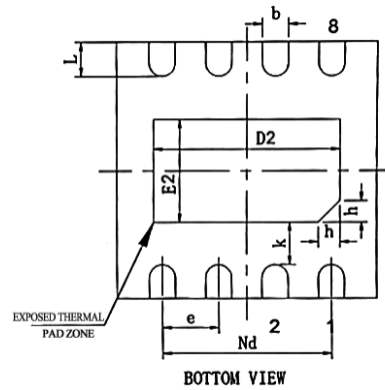
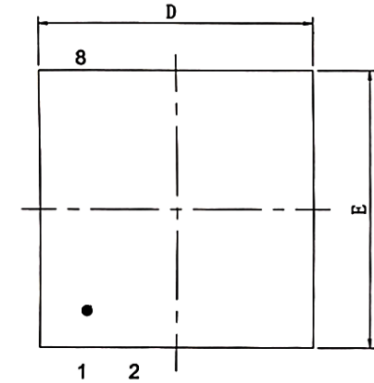


LAND PATTERN EXAMPLE (Unit: mm)

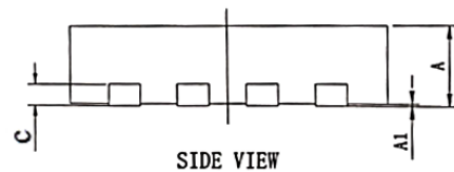


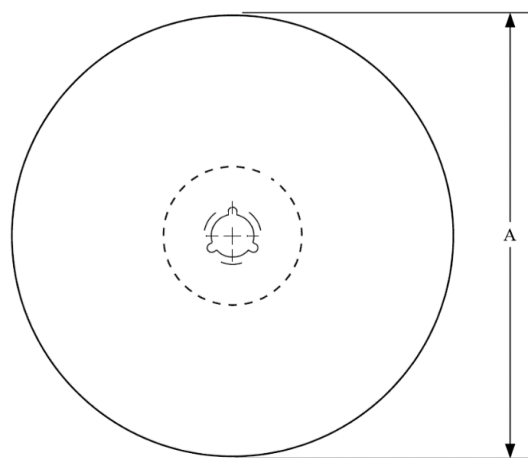
**DFN3\*3-8 DIMENSIONS**
**PACKAGE SIZE**

SYMBOL	MIN/mm	TYP /mm	MAX/mm
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3	0.203 REF		
D	2.90	3.00	3.10
E	2.90	3.00	3.10
D2	2.05	2.15	2.25
Nd	1.95BSC		
E2	1.10	1.20	1.30
b	0.25	0.30	0.35
e	0.65 TYP		
k	0.50REF		
L	0.35	0.4	0.45
h	0.20	0.25	0.30

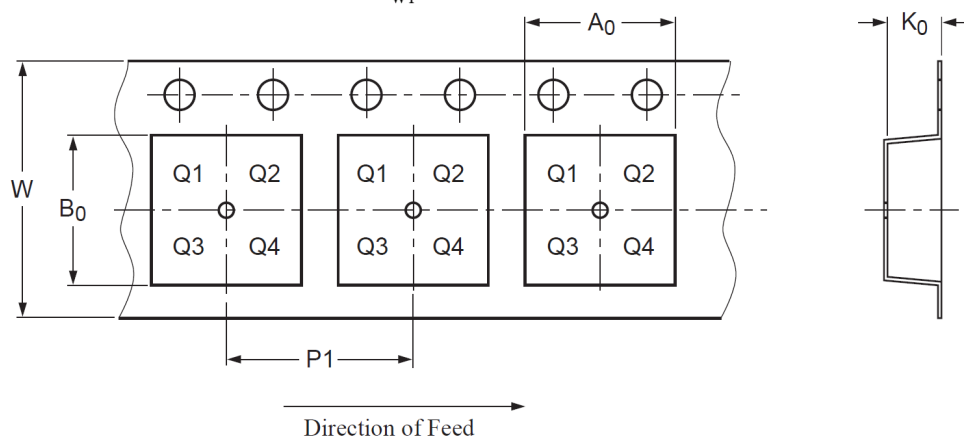
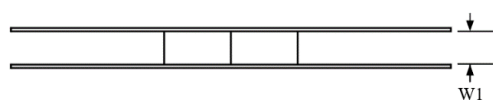


LAND PATTERN EXAMPLE (Unit: mm)



**TAPE AND REEL INFORMATION**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



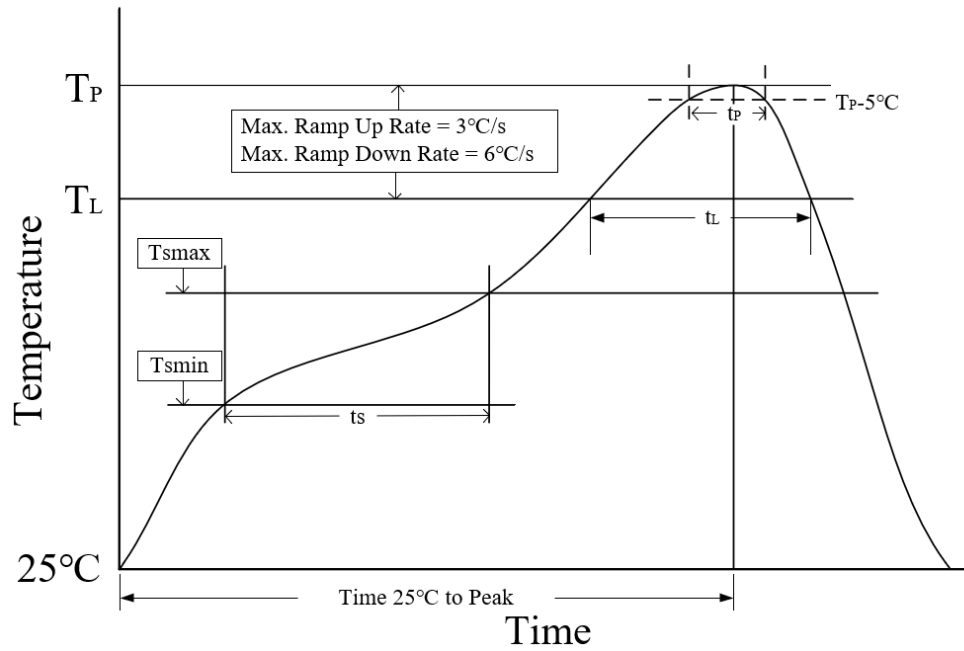
PIN1 is in quadrant 1

Package Type	Reel Diameter A (mm)	Tape width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)
SOP8	330 $\pm$ 1	12.4	6.60 $\pm$ 0.1	5.30 $\pm$ 0.10	1.90 $\pm$ 0.1	8.00 $\pm$ 0.1	12.00 $\pm$ 0.1
DFN3*3-8	329 $\pm$ 1	12.4	3.30 $\pm$ 0.1	3.30 $\pm$ 0.1	1.10 $\pm$ 0.1	8.00 $\pm$ 0.1	12.00 $\pm$ 0.3

**ORDERING INFORMATION**

TYPE NUMBER	PACKAGE	PACKING
SIT1051AQT	SOP8	Tape and reel
SIT1051AQT/E	SOP8	Tape and reel
SIT1051AQT/3	SOP8	Tape and reel
SIT1051AQTk/3	DFN3*3-8, small shape, no leads, 8 terminals	Tape and reel

SOP8 is packed with 2500 pieces/disc in braided packaging. Leadless DFN3\*3-8 is packed with 6000 pieces/disc in braided packaging.

**REFLOW SOLDERING**


Parameter	Lead-free soldering conditions
Ave ramp up rate ( $T_L$ to $T_P$ )	$3^\circ\text{C/second max}$
Preheat time $t_s$ ( $T_{smin}=150^\circ\text{C}$ to $T_{smax}=200^\circ\text{C}$ )	60-120 seconds
Melting time $t_L$ ( $T_L=217^\circ\text{C}$ )	60-150 seconds
Peak temp $T_P$	$260-265^\circ\text{C}$
$5^\circ\text{C}$ below peak temperature $t_p$	30 seconds
Ave cooling rate ( $T_P$ to $T_L$ )	$6^\circ\text{C/second max}$
Normal temperature $25^\circ\text{C}$ to peak temperature $T_P$ time	8 minutes max

**Important statement**

SIT reserves the right to change the above-mentioned information without prior notice.

**REVISION HISTORY**

Version number	Data sheet status	Revision Date
V1.0	Initial version.	August 2022
V1.1	Updated package dimension schematic (size unchanged); Added AEC-Q100 qualified.	March 2023